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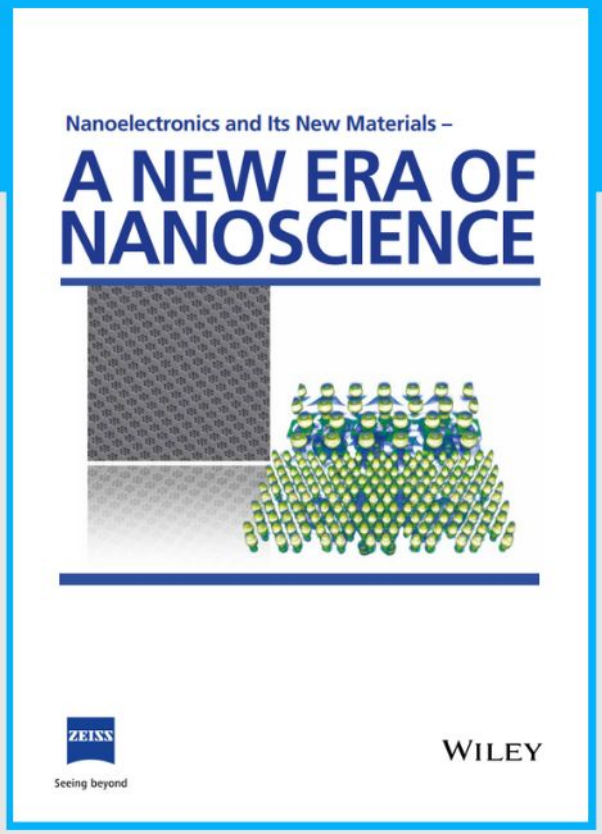

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High-Performance CMOS Inverter Array with Monolithic 3D Architecture Based on CVD-Grown n-MoS_2 and p-$MoTe_2$

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In this work, monolithic three-dimensional complementary metal oxide semiconductor (CMOS) inverter array has been fabricated, based on large-scale n-MoS_2 and p-$MoTe_2$ grown by the chemical vapor deposition method. In the CMOS device, the n- and p-channel field-effect transistors (FETs) stack vertically and share the same gate electrode. High *k* HfO_2 is used as the gate dielectric. An Al_2O_3 seed layer is used to protect the MoS_2 from heavily n-doping in the later-on atomic layer deposition process. P-$MoTe_2$ FET is intentionally designed as the upper layer. Because p-doping of $MoTe_2$ results from oxygen and water in the air, this design can guarantee a higher hole density of $MoTe_2$. An HfO_2 capping layer is employed to further balance the transfer curves of n- and p-channel FETs and improve the performance of the inverter. The typical gain and power consumption of the CMOS devices are about 4.2 and 0.11 nW, respectively, at V_{DD} of 1 V. The statistical results show that the CMOS array is with high device yield (60%) and an average voltage gain value of about 3.6 at V_{DD} of 1 V. This work demonstrates the advantage of two-dimensional semi-conductive transition metal dichalcogenides in fabricating high-density integrated circuits.

1. Introduction

The complementary metal oxide semiconductor (CMOS) inverter is one of the most significant electronic devices, in which the n-channel field-effect transistor (n-FET) and p-channel FET (p-FET) are two basic components. Moore's Law demands incessantly increasing device density in integrated circuits (ICs). Current microelectronic techniques are approaching the semiconductor process limit. Besides, the channel length in FET cannot be shortened ceaselessly because of the short channel effect.[1,2] Increasing transistor packing density by fabricating multilayer devices to build monolithic three-dimensional (3D) integration is another way to increase device density in ICs.[3,4]

Two-dimensional (2D) semi-conductive transition metal dichalcogenides (TMDCs), such as MoS_2 and $MoTe_2$, etc., have lots of advantages in preparing monolithic 3D integrated devices. Large-scale MoS_2 and $MoTe_2$ films can be synthesized by the chemical vapor deposition (CVD) method.[5,6] The as-grown MoS_2 and $MoTe_2$ usually behave as n- and p-type semiconductive property, respectively. The p-type of $MoTe_2$ results from oxygen and water in the air.[7,8] Their atomic thickness and suitable bandgap (1–2 eV) facilitate effective electrostatic control and deep-submicrometer interconnect.[9,10] Besides, TMDCs, free from covalent bonds or dangling bonds between neighbored layers,[11] are easy to be stacked layer by layer vertically without the requirement of lattice matching.[12] Moreover, the TMDCs have larger in-plane and smaller out-of-plane thermal conductivity, which can reduce lateral thermal resistance and self-heating from the neighbored layers as well as the power dissipation.[13] To the best of our knowledge, so far, most reported TMDCs-based CMOS inverters are made from mechanically exfoliated materials.[14–20] For practical application, fabricating large-scale device array with good uniformity is indispensable. In 2019, Jiao's group demonstrated bilayer p-FETs with vertical interconnections.[21] TMDCs-based 3D integrated CMOS inverter was first demonstrated in 2016 using mechanically exfoliated n-MoS_2 and p-WSe_2 channel materials.[4] Recently, vertical stacking CMOS inverter array was reported, where

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CVD-grown n-MoS_2 and p-$MoTe_2$ were used as upper and bottom channel materials, respectively. Among 25 devices, 7 ones are functional, corresponding to 28% device yield. The average voltage gain is about 1.53 at V_{DD} of 1 V. Notably, tri-layer MoS_2 was used in that work, which requires multiple transfer processes. It is well known that power consumption is another important criterion for CMOS device. However, no power consumption data was provided in that work.[22]

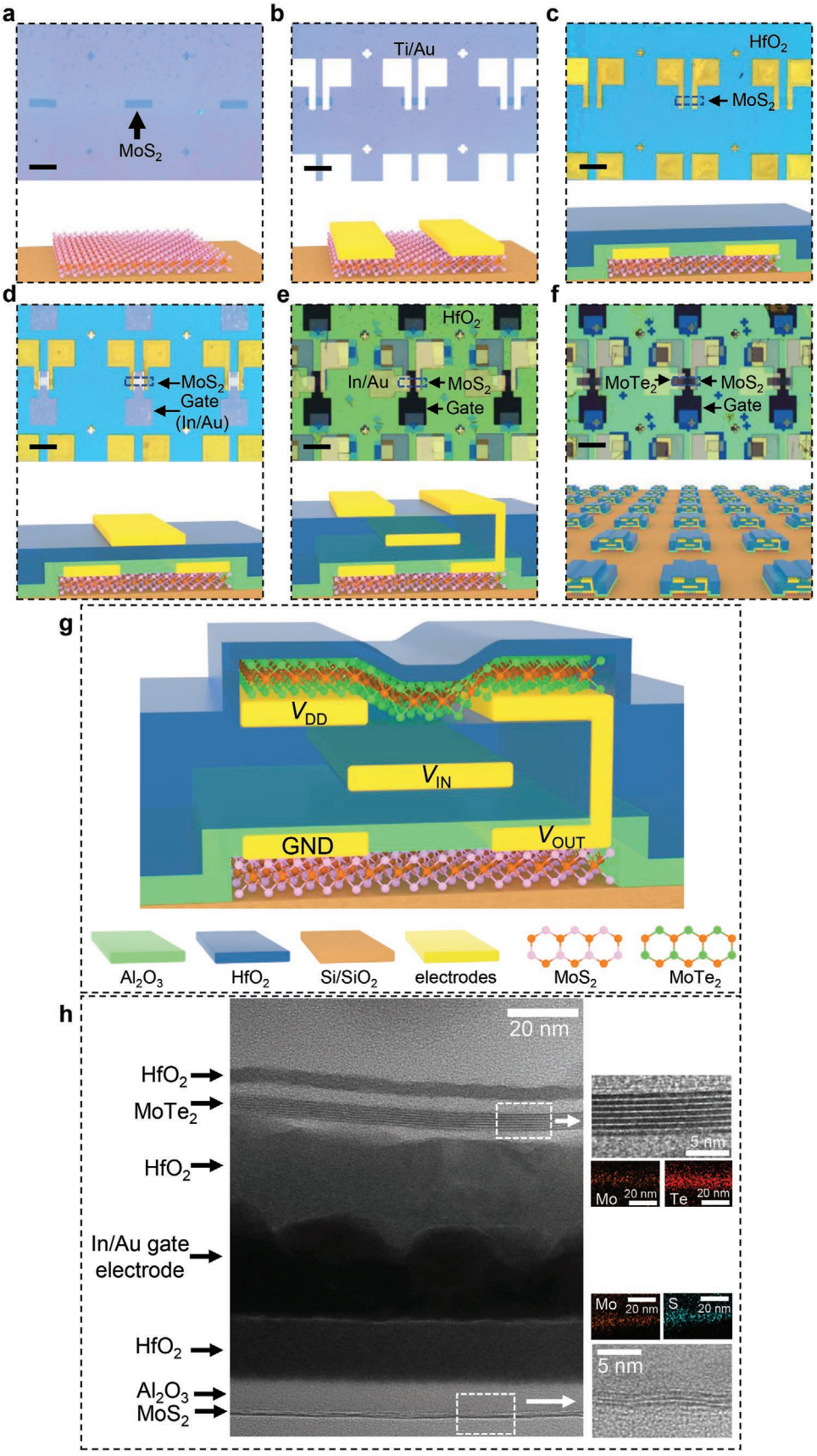
Previously, our group successfully synthesized large-scale single crystalline MoS_2 and $MoTe_2$ via CVD method.[23–27] We also developed a method of transferring CVD-grown $MoTe_2$ using only deionized water to reduce the chemical residues.[28] In this work, we have fabricated monolithic 3D integrated CMOS inverter array based on CVD-grown large-scale n-MoS_2 and p-$MoTe_2$ film. In the CMOS device, the n- and p-FETs stack vertically and share the same gate electrode. High k HfO_2 is used as the gate dielectric layer. An Al_2O_3 seed layer is used to protect the MoS_2 from heavily n-doping of the later-on atomic layer deposition (ALD) process.[8,17,27,29–33] It is worth noting that we intentionally design the p-$MoTe_2$ FET as the upper layer. Because p-doping of $MoTe_2$ results from oxygen and water in the air,[7,8] this design can guarantee a higher hole density of $MoTe_2$. Moreover, the upper layer few-layer $MoTe_2$ is transferred in one step, which simplifies the device fabrication process, and may improve the device yield. The statistical results show that the as-fabricated inverter array is with high device yield (60%) and an average voltage gain value of about 3.6 at V_{DD} of 1 V. In addition, a HfO_2 capping layer is employed to further improve the performance of the inverter. By controlling the HfO_2 thickness and the ALD condition, we can moderate the hole density in the p-channel to make it more matched with the electron density in the n-channel, and therefore balance the transfer curves of the n-MoS_2 and p-$MoTe_2$ FETs, which favors realizing zero-point symmetry voltage transfer characteristics (VTCs) of the inverter. With this approach, we have markedly increased the gain and reduced the power consumption of the devices. Overall, our devices present clear VTCs with typical voltage gain and power consumption to be about 4.2 and 0.11 nW, respectively, at V_{DD} of 1 V, which are the best results among the so-far reported CMOS inverter devices based on CVD-grown TMDCs, and even competitive compared to their mechanically exfoliated TMDCs counterparts, under similar power consumption (<1 nW) and measurement condition (in dark, room temperature). Our work demonstrates that TMDCs have a bright future in making high-performance and high-density electronic devices in ICs.

2. Result and Discussion

The optical images of the CVD-grown n-MoS_2 used in this work are shown in Figure S1a,b, Supporting Information. The n-MoS_2 film is formed by triangular single-crystal MoS_2 domains with a typical side length of about 50 µm. The Raman spectrum of as-grown MoS_2 is shown in Figure S1c, Supporting Information, which consists of strong in-plane E^1_{2g} (380.9 cm^{-1}) and out-of-plane A_{1g} (401.3 cm^{-1}) modes. The distance between them is about 20.4 cm^{-1}. The full width at half maximum (FWHM) of E^1_{2g} is about 3.9 cm^{-1}, close to that of exfoliated monolayer MoS_2 flake (3.7 cm^{-1}).[34] The thickness of MoS_2 film is about 0.8 nm, characterized by atomic force microscopy (Figure S1e, Supporting Information). These results indicate that the n-MoS_2 film is monolayer with high crystal quality. The electrical property of MoS_2 is characterized by fabricating FET. The transfer curve of the MoS_2 FET (Figure S1d, Supporting Information) presents n-type channel behavior with on/off ratio of 1.3×10^6. The obtained electron density and field-effect mobility are about 1.5×10^{12} cm^{-2} and 10.7 $cm^2V^{-1}s^{-1}$, respectively.

The optical images of the CVD-grown p-$MoTe_2$ used in this work are shown in Figure S2a,b, Supporting Information. The p-$MoTe_2$ film is formed by circular single-crystal 2H-$MoTe_2$ domains.[26,27] Notably, the $MoTe_2$ single crystal domain can be as large as wafer scale under specific growth conditions.[35] The Raman spectra of $MoTe_2$ before and after transfer process are shown in Figure S2c, Supporting Information. Both of them consist of a strong in-plane E^1_{2g} (232.9 cm^{-1}) mode together with a weak out-of-plane A_{1g} (172.8 cm^{-1}) mode. The FWHM of E^1_{2g} mode for the as-grown $MoTe_2$ is about 4.2 cm^{-1}, which is close to 3.3 cm^{-1} of mechanically exfoliated $MoTe_2$, confirming the formation of high-quality $MoTe_2$.[27,36] The FWHM of E^1_{2g} mode for the transferred $MoTe_2$ increases little (≈4.8 cm^{-1}), indicating the quality of p-$MoTe_2$ changes little after the transfer process. The $MoTe_2$ film is about 5.6 nm thick (corresponding to 7-layer $MoTe_2$) (Figure S2e, Supporting Information). The transfer curve of the $MoTe_2$ FET (Figure S2d, Supporting Information) presents p-type channel behavior with on/off ratio of about 3.9×10^3. The obtained hole density and field-effect mobility are about 1.2×10^{12} cm^{-2} and 6.7 $cm^2V^{-1}s^{-1}$, respectively.

Figure 1a–f are schematic diagrams of the fabrication processes of the CMOS inverter array with monolithic 3D architecture, along with the corresponding optical images. First, large-scale monolayer n-MoS_2 film were grown on p^+-Si/SiO_2 (285 nm) substrate via CVD method (Figure S1, Supporting Information), and patterned into rectangular channels (Figure 1a). Then, Ti/Au (10/50 nm) source and drain electrodes were fabricated at two ends of each n-MoS_2 channel, followed by an annealing process for better contact between the electrodes and n-MoS_2 (Figure 1b). The channel length and width of each n-FET are both 30 µm. Notably, in order to protect the MoS_2 from heavily n-doping of the later-on ALD process,[30] we pre-evaporated a thin layer of Al_2O_3 seed layer (8 nm in this work) using electron-beam (E-beam) evaporation.[32,33] Next, a layer of HfO_2 gate dielectric (20 nm) for n-MoS_2 FETs was deposited by ALD (Figure 1c), and arrayed In/Au (10/20 nm) gate electrodes were fabricated on it (Figure 1d). After that, another layer of HfO_2 gate dielectric (30 nm) and In/Au (10/40 nm) source and drain electrodes for p-$MoTe_2$ FETs were fabricated (Figure 1e). The p-$MoTe_2$ FET shares the same gate electrode with the n-MoS_2 FET. It is worth noting that, in a CMOS device, the drains of n- and p-FETs should be connected. Therefore, before the In/Au electrodes were evaporated, holes penetrating through HfO_2 and Al_2O_3 layers were made via UV lithography and argon ion etching. After all these processes, CVD-grown p-$MoTe_2$ was transferred on the target substrate, and patterned into rectangle channels. The channel length and width of each p-FET are 20 and 30 µm, respectively.



Finally, a 5 nm HfO_2 capping layer was deposited to reduce the hole density of p-$MoTe_2$, and balance the transfer curves of the n- and p-FETs. It is worth noting that the 5 nm HfO_2 ALD process also has an annealing effect to the bottom n-MoS_2 FET, making it more balanced with the upper p-$MoTe_2$ FET. The cross-section of a representative CMOS inverter was characterized by high-resolution transmission electron microscopy (HR-TEM). The HR-TEM image (Figure 1h) demonstrates distinct layered structure of the device. The zoom-in images at MoS_2 and $MoTe_2$ regions, together with the corresponding energy dispersive spectroscopy (EDS) elemental mapping images (the inset in Figure 1h) confirm the high-quality of mono-layer MoS_2 and few-layer $MoTe_2$ even after the transfer process. The cross-sectional high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image and spatial distributions of Au, Hf, and Al are shown in Figure S3, Supporting Information, which also shows distinct layered structures of the 3D device.

The electrical properties of the n- and p-FET components were characterized after fabricating the CMOS inverter array. The representative results are shown in **Figure 2**. Both n-MoS_2 and p-$MoTe_2$ FETs have small off-state current. The on/off ratios of n- and p-FETs are about 10^6 and 10^5, respectively. Notably, the transfer curves of them have an intersection at 0.03 V, very close to 0 V, which favors realizing zero-point symmetry VTC of the inverter. Besides, the current magnitude at the intersection is only about 1.0×10^{-10} A, guaranteeing a very low working current and power consumption of the inverter.

Figure 3a shows the VTC and voltage gain (the maximum value of $\left(-\frac{d\,V_{OUT}}{d\,V_{IN}}\right)$) plots of the inverter at various V_{DD}. The corresponding CMOS inverter circuit diagram is plotted in the inset. Herein, the source of n-FET is grounded, and the source of p-FET serves as the supply voltage electrode (V_{DD}). The gate and the drains of n- and p-FETs serve as the input voltage (V_{IN}) and output voltage (V_{OUT}) electrodes, respectively. For each applied V_{DD}, the VTC shows clear logic swing with voltage gain larger than 1, satisfying the requirement of logic application. The voltage gain is as high as 4.2 and 33.0 at V_{DD} of 1 and 4 V, respectively, close to those of the CMOS inverters made of mechanical exfoliated TMDCs.[14,15,18] Figure 3b shows the power consumption ($V_{DD} \times I_{DD}$) characteristics of this device. The peak power consumption is as low as 0.11 nW at V_{DD} of 1 V. A summary of the key parameters of the so-far reported TMDC-based CMOS inverters is shown in **Table 1**.

In order to verify the effect of the HfO_2 capping layer, we compared the performances of an inverter with and without the capping layer (Figure S4, Supporting Information). We can see (Figure S4a, Supporting Information) that, after being deposited the 5 nm HfO_2, the on-state current of the n-MoS_2 FET increases from 2.5×10^{-6} to 5.8×10^{-6} A due to the annealing effect during the ALD process,[28,37,38] which improves the contact between n-MoS_2 and metal electrodes. On the contrary, the ALD process-induced n-type doping effect causes the on-state current of the p-$MoTe_2$ FET decreases from 1.7×10^{-6} to 1.3×10^{-8} A. As a result, the current magnitude at the intersection of the two transfer curves reduces from 1.4×10^{-8} to 3.1×10^{-10} A, leading to a lower power consumption of the inverter. Figure S4b shows the VTC together with the voltage gain plot. Figure S4c shows the power consumption characteristics of the CMOS inverter. After being deposited the 5 nm HfO_2 capping layer, the voltage gain increases from 1.9 (3.6) to 2.8 (9.5), while the peak power consumption decreases from 13.01 (74.94) nW to 0.32 (2.92) nW, at V_{DD} of 1 V (2 V). We also performed statistical analysis on more devices. The voltage gains and power consumptions of fourteen participating devices are presented in Figure S4d,e, Supporting Information, respectively. The statistics verify again that the gain increases markedly, and power consumption decreases dramatically after the ALD of 5 nm HfO_2 capping layer.

We also investigated the dynamic switching behavior of the CMOS inverters. Herein, the inverter was driven by square wave V_{IN} with various frequencies (F). The high and low levels of V_{IN} are 3 and −3 V, respectively. **Figure 4**a,b show the time-dependent V_{IN} and V_{OUT} under F of 100 and 800 Hz, respectively. We can see that the logic switching behavior is clear at 100 Hz and remains to be observed at 800 Hz. The rising time (t_r) and falling time (t_f) are 397 and 372 µs, respectively, at 800 Hz, calculated at 10% and 90% of V_{OUT} amplitude in Figure 4b (marked by the red dashed lines).

The statistical data of voltage gain and power consumption from thirty CMOS inverters in the device array are presented in **Figure 5**a,b, respectively. Among the 30 devices, 18 work normally, corresponding to 60% device yield. At V_{DD} = 1 V, the average voltage gain is about 3.6. The lowest and highest values are 2.0 and 5.4, respectively. All of them satisfy the requirement of logic application. Significantly, the average power consumption of the devices is as low as 0.17 nW. The highest and lowest values are 0.43 and 0.04 nW, respectively. The optical image containing all the devices in the array is shown in Figure 5c. We can see that in some devices (circled by the white dotted lines), $MoTe_2$ channels are missing. The possible reasons are: 1. During the $MoTe_2$ transfer process, some cracks and holes were introduced;[39–41] 2. During the photoresist removal process after reactive ion etching the $MoTe_2$ channels, certain $MoTe_2$ channels were torn off the substrate.

Figure 1. a–f) Schematic diagrams of the fabrication processes of the monolithic 3D architecture CMOS inverter array along with corresponding optical images. a) Large-scale monolayer n-MoS_2 film were grown on p^+-Si/SiO_2 (285 nm) substrate using CVD method and patterned into rectangluar channels. b) Pairs of Ti/Au (10/50 nm) source and drain electrodes were fabricated at two ends of each n-MoS_2 channel, followed by an annealing process for better contact between the electrodes and n-MoS_2. The channel length and width of each n-FET are both 30 µm. c) 8 nm Al_2O_3 was deposited by E-beam evaporation, followed by ALD of 20 nm HfO_2 dielectric. d) Arrayed In/Au (10/20 nm) electrodes were fabricated, which served as gate electrodes for both n-MoS_2 and p-$MoTe_2$ FETs. e) A layer of HfO_2 gate dielectric (30 nm) for p-$MoTe_2$ FETs was deposited and holes were etched through HfO_2 and Al_2O_3 layers. Then In/Au (10/40 nm) source and drain electrodes of p-$MoTe_2$ FETs were fabricated. After these processes, the drain electrodes of n- and p-FETs are contacted. f) A CVD-grown $MoTe_2$ film was transferred onto the substrate and patterned into rectangular channels. The channel length and width of each p-FET are 20 and 30 µm, respectively. Finally, a layer of 5 nm HfO_2 capping layer was deposited via ALD. Scale bars in a) – f) are 100 µm. g) Schematic diagram of the CMOS inverter. h) HR-TEM image of the 3D inverter. Inset: The zoom-in images at MoS_2 and $MoTe_2$ regions, together with the corresponding EDS elemental mapping images.

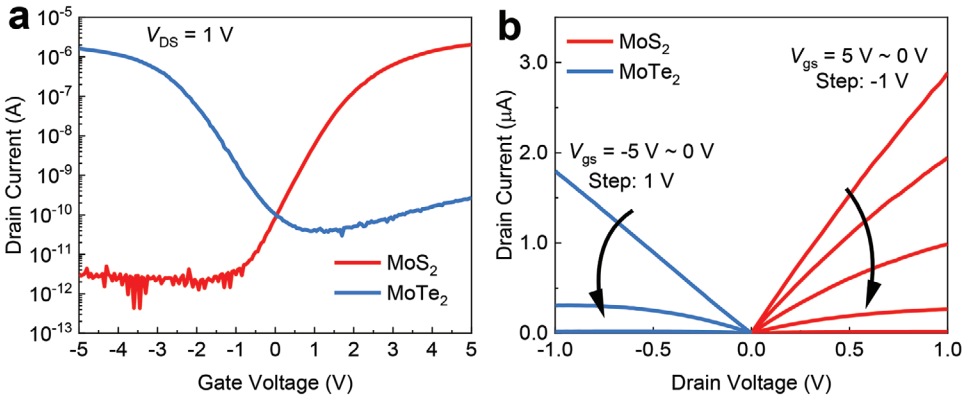


Figure 2. a) The transfer curves of n-MoS_2 and p-$MoTe_2$ FETs in an inverter. b) $I_D - V_D$ curves of n-MoS_2 FET (red lines) and p-$MoTe_2$ FET (blue lines) with various gate voltage (V_{gs}).

3. Conclusions

We have fabricated large-scale CMOS inverter array using CVD-grown n-MoS_2 and p-$MoTe_2$. In the device, the n- and p-channel FETs stack vertically and share the same gate. Our devices present clear voltage transfer characteristics with performance comparable or even better than their counterparts fabricated by mechanically exfoliated TMDCs. The statistical results show that the as-fabricated CMOS inverter array is with high device yield (60%). We attribute our achievement to the high-quality CVD-grown materials, the improved $MoTe_2$ transfer process, and the balanced n- and p-channel currents. We think the device yield can further be improved by directly growing $MoTe_2$ on the target substrate, which can avoid mechanical damages from the transfer process, and enhance the interaction between the $MoTe_2$ film and the target substrate. Our work demonstrates the feasibility of fabricating high-performance and high-density monolithic 3D integrated CMOS device array using TMDCs, which may find application in semiconductor ICs.

4. Experimental Section

Synthesis of MoS_2: Monolayer MoS_2 was grown by a CVD method in a 3-temperature-zone system using S powder and MoO_3 powder as sources, perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt as seeding promoter, pieces of p^+-Si/SiO_2 (285 nm) wafer as substrates, and high-purity argon as carrier gas. S powder, MoO_3 powder, and the substrates were placed in quartz boats, which were later inserted into a one-inch diameter quartz tube inside a tube furnace in sequence from upstream to downstream of argon carrier gas. The temperatures for S and MoO_3 sources were 160 and 650 °C, respectively. The growth duration was 5 min. After the growth, the furnace was cooled down to room temperature naturally. During the whole process, the argon flow rate was kept at 15 standard cubic centimeters per minute (sccm).

Synthesis of $MoTe_2$: The $MoTe_2$ film was grown by tellurizing Mo film in a tube furnace. First, Mo film was deposited on p^+-Si/SiO_2 (285 nm) substrate using radio frequency magnetron sputtering. The substrates and Te powders were placed in a quartz boat, which was later inserted into a one-inch diameter quartz tube inside the furnace with Te powders at upstream of carrier gas. First, the quartz tube was evacuated to less than 10 mTorr. Second, high-purity Ar gas was let in at a rate of 500 sccm until atmospheric pressure was reached. Then Ar and H_2 were let in at flow rates of 5 and 7 sccm, respectively. Next, the furnace temperature was ramped to 630 °C and kept there for 3 h. After the growth, the furnace was cooled down to room temperature naturally.

Transfer Process of $MoTe_2$: A layer of polymethyl methacrylate (PMMA) was spin-coated on a substrate with a $MoTe_2$ film at 2000 revolutions per minute for 60 s and heated on a hot plate at 170 °C for 3 min. Both the PMMA and $MoTe_2$ film at the edge of the substrate were scraped off by a tweezer. With the help of a tweezer, the substrate was slowly dipped into deionized water, starting from the corner, until the whole sample was immersed. Due to the surface energy imbalance between $MoTe_2$

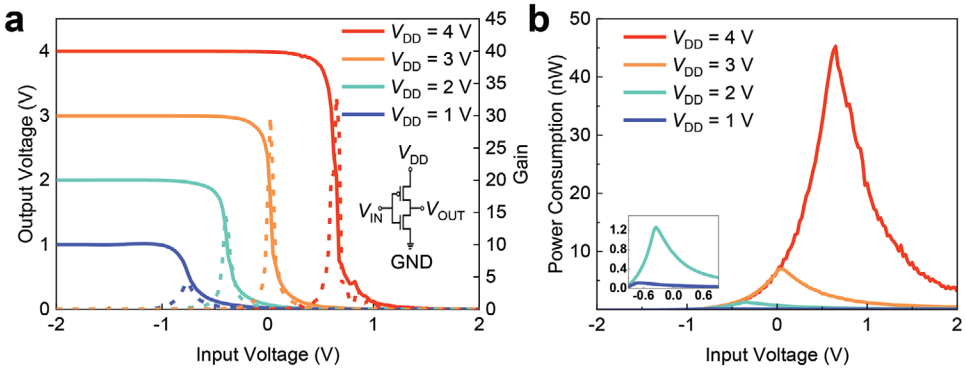


Figure 3. a) The VTC and voltage gain plots of the inverter at various V_{DD}. The solid lines represent $V_{OUT} - V_{IN}$ curves and the dashed lines represent the voltage gain plot. Inset: the circuit diagram of a CMOS inverter. b) The power consumption characteristics of the inverter at various V_{DD}. Peak power consumption is 0.11 nW at V_{DD} = 1 V. Inset: The zoom-in figure at V_{DD} of 1 and 2 V.

Table 1. A summary of the voltage gains and power consumptions together with the device structures and measurement conditions of the so-far reported TMDC-based CMOS inverters.

Channel materials	V_{DD} [V]	Peak power consumption [nW]	Gain	Structure	Measurement environment	Ref.
CVD p-$MoTe_2$ and n-MoS_2	1	0.11	4.2	Monolithic 3D architecture	Dark Room temperature	This work
CVD p-$MoTe_2$ and n-MoS_2	1	Not provided	1	Monolithic 3D architecture	Dark Room temperature	[22]
Ex. p-WSe_2 and n-MoS_2	3	Not provided	10	Monolithic 3D architecture	Dark Room temperature	[4]
CVD p-$MoTe_2$ and n-MoS_2	1	0.37	≈2	Planar CMOS	Dark Room temperature	[28]
Ex. p-$MoTe_2$ and n-MoS_2	0.25	0.4	3.5	Planar CMOS	Dark Room temperature	[14]
Ex. p-$MoTe_2$ and n-MoS_2	1	4	≈5	Planar CMOS	Dark Room temperature	[15]
Ex. p-$MoTe_2$ and n-MoS_2	3	~400	55.16	Planar CMOS	Dark Room temperature	[19]
Ex. p-WSe_2 and n-MoS_2	1	$\approx 1 \times 10^3$	≈3	Planar CMOS	Dark Room temperature	[18]
Ex. p-WSe_2 and n-MoS_2	5	1	23	Planar CMOS	Dark Room temperature	[16]
Ex. p-$MoTe_2$ and n-$MoTe_2$ (n-doped)	1	5	≈18	Planar CMOS	Dark Room temperature	[17]
CVD p-WSe_2 and n-MoS_2	0.1	0.3	3.1	Planar CMOS	N_2-filled glove box Room temperature	[10]
Ex. p-WSe_2 and n-MoS_2	2	0.068	≈12	Planar CMOS	Low pressure environment (10^{-5} bar) Room temperature	[20]

Ex., mechanically exfoliated; CVD, CVD-grown.

film and substrate, deionized water entered the gap between them and lifted off the PMMA/$MoTe_2$ film from the substrate. The PMMA/$MoTe_2$ film, which floated on the water, was transferred to the target substrate. After a naturally drying process, the PMMA was dissolved by acetone, and $MoTe_2$ was left on the target substrate.

Fabrication of Monolithic 3D Inverter Array: Both the $MoTe_2$ and MoS_2 films were patterned into rectangular sheets through ultra-violet (UV) lithography and reactive ion etching. The Ti/Au electrodes were fabricated by UV lithography, E-beam evaporation, and lift-off process. The temperature and time for the annealing process were 300 °C and 60 min, respectively, in a low-pressure environment with Ar and H_2 gas. The In/Au electrodes were fabricated by UV lithography, thermal evaporation, and lift-off process. The Al_2O_3 and HfO_2 layers were deposited by E-beam evaporation and ALD, respectively. In the ALD process, tetrakis (dimethylamido) hafnium and deionized water served as precursors and high-purity N_2 served as carrier gas. The reaction temperature for HfO_2 dielectric layer (20 nm) of n-MoS_2 FETs was 105 °C, and that for HfO_2 dielectric layer (30 nm) and capping layer

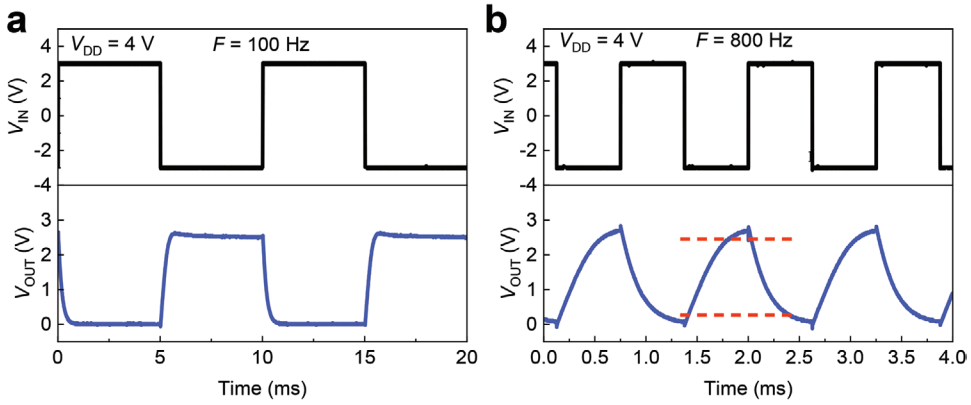


Figure 4. The dynamic switching behavior of the CMOS inverter. Herein, V_{IN} is square wave changing between −3 and 3 V with various frequencies (F). a) and b) are time-dependent V_{IN} and V_{OUT} under 100 and 800 Hz, respectively. Logic switching behavior is clear at 100 Hz and remains to be observed at 800 Hz. The rising time (t_r) and falling time (t_f) are 397 and 372 µs, respectively, at 800 Hz, calculated at 10% and 90% of V_{OUT} amplitude (marked by the red dashed lines).

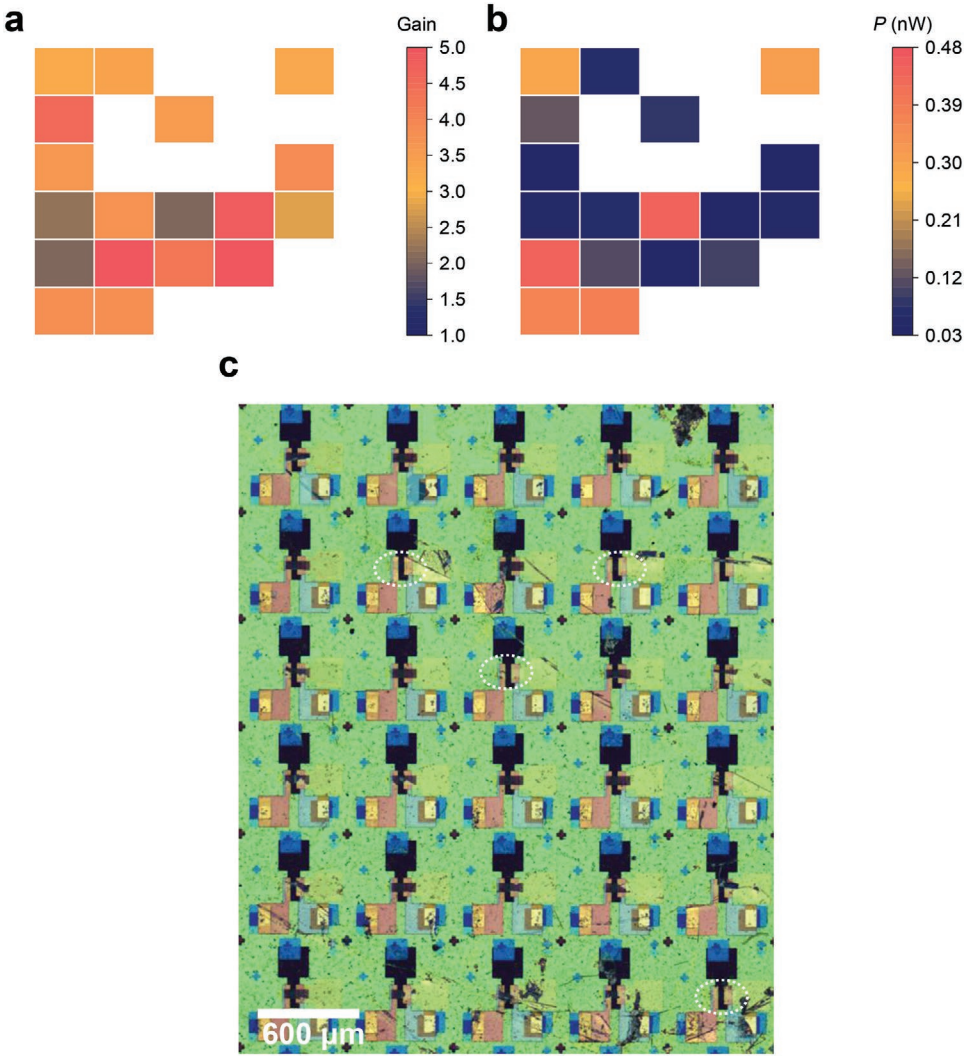


Figure 5. The statistical data of a) voltage gain and b) power consumption at V_{DD} = 1 V from 30 CMOS inverters in the device array. c) The optical image containing all the devices in the array. In some devices (circled by the white dotted lines), the $MoTe_2$ channels are missing.

(5 nm) of p-$MoTe_2$ FETs was 90 °C. The HfO_2 thickness was controlled by deposition time. The holes penetrating through HfO_2 and Al_2O_3 layers for measuring purpose were fabricated via UV lithography and argon ion etching.

Characterizations: Both optical images and Raman spectra were collected by micro-zone confocal Raman system (WITec alpha 300R) attached with a 532 nm laser. The sample for HAADF-STEM observation is prepared by a focused ion beam system (ThermoFisher Helios G4 UX). The HR-TEM was carried out using a transmission electron microscope (FEI Tecnai F20) with an acceleration voltage of 200 kV. The HAADF-STEM and EDS elemental mapping images were taken by another transmission electron microscope (FEI Tecnai F30) with an acceleration voltage of 300 kV. The thicknesses of MoS_2 and $MoTe_2$ were measured by an atomic force microscope (Asylum Research, Cypher S). The electrical measurements were conducted in a probe station which was connected to a semiconductor characterization system (Keithley 4200A-SCS). For the dynamic switching performance measurement, a function generator (Tektronix AFG 3102) and a digital oscilloscope (Tektronix DPO 2024) were employed to generate the V_{IN} and record the V_{OUT}, respectively. Both the function generator and the digital oscilloscope had common ground with the semiconductor characterization system, which provided the V_{DD}. All the characterizations were performed in dark and room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

3D integration, complementary metal oxide semiconductor (CMOS) inverter, n-MoS_2 and p-$MoTe_2$, power consumption, voltage gain

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