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A native oxide high-κ gate dielectric for two-dimensional electronics

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Silicon-based transistors are approaching their physical limits and thus new high-mobility semiconductors are sought to replace silicon in the microelectronics industry. Both bulk materials (such as silicon-germanium and III–V semiconductors) and low-dimensional nanomaterials (such as one-dimensional carbon nanotubes and two-dimensional transition metal dichalcogenides) have been explored, but, unlike silicon, which uses silicon dioxide (SiO_2) as its gate dielectric, these materials suffer from the absence of a high-quality native oxide as a dielectric counterpart. This can lead to compatibility problems in practical devices. Here, we show that an atomically thin gate dielectric of bismuth selenite (Bi_2SeO_5) can be conformally formed via layer-by-layer oxidization of an underlying high-mobility two-dimensional semiconductor, Bi_2O_2Se. Using this native oxide dielectric, high-performance Bi_2O_2Se field-effect transistors can be created, as well as inverter circuits that exhibit a large voltage gain (as high as 150). The high dielectric constant (~21) of Bi_2SeO_5 allows its equivalent oxide thickness to be reduced to 0.9 nm while maintaining a gate leakage lower than thermal SiO_2. The Bi_2SeO_5 can also be selectively etched away by a wet chemical method that leaves the mobility of the underlying Bi_2O_2Se semiconductor almost unchanged.

Since the invention of integrated circuits in the late 1950s[1], silicon has been the dominant semiconductor for microelectronics. In addition to its moderate bandgap, excellent chemical stability and abundance in the lithosphere, silicon benefits from having a native oxide—silicon dioxide (SiO_2). Highly dense and uniform layers of SiO_2, obtained from thermal oxidation of silicon, can serve as a hard mask to protect silicon wafers from contamination and also as the gate dielectric in silicon field-effect transistors (FETs) because of its insulating properties and the excellent interface quality between silicon and SiO_2 (refs. [2,3]). Selective etching of SiO_2 over silicon further allows the microfabrication of complicated integrated circuits[4].

However, silicon-based FETs face various challenges at sub-10-nm nodes, the most prominent of which are reduced mobility and increased short-channel effects[5]. It is thus desirable to develop high-mobility semiconductors to replace silicon as devices are further scaled in line with Moore's law. Possible materials for this challenge include SiGe[6], Ge[7], III–V semiconductors[8] and two-dimensional (2D) electron gas systems[9] such as $LaAlO_3/SrTiO_3$. High-mobility low-dimensional semiconductors such as 1D carbon nanotubes[10,11], 2D transition metal dichalcogenides[12], 2D black phosphorus[13] and 2D InSe[14], also have potential to extend Moore's law by suppressing short-channel effects due to their atomically thin structures[15–19]. However, none of these materials can challenge the dominance of silicon in microelectronics, partly due to the lack of a stable native oxide that is compatible with the semiconductor[20,21]. Although much effort has been made on the oxides of SiGe[22], Ge[23], III–V semiconductors[24], 2D MoS_2 (ref. [25]), 2D TaS_2 (ref. [26]), 2D HfS_2 (ref. [27]), 2D WSe_2 (ref. [28]), 2D $HfSe_2$ and $ZrSe_2$ (ref. [29,30]), the oxides of these materials are generally non-stoichiometric and highly defective at the oxide–semiconductor interface. A semiconductor and its native oxide that rivals the performance of Si/SiO_2 has yet to be found.

In this Article, we show that atomically thin dielectric layers of bismuth selenite (Bi_2SeO_5) can be conformally formed through layer-by-layer oxidation of the underlying 2D Bi_2O_2Se semiconductor at elevated temperatures, ensuring an atomically sharp and chemically clean interface. Due to its high dielectric constant ($\varepsilon_r \approx 21$), and good band alignment with the semiconductor, the insulating Bi_2SeO_5 can directly serve as an ideal gate dielectric for Bi_2O_2Se FETs. The resulting devices exhibit high apparent field-effect mobilities of $>300\,cm^2\,V^{-1}\,s^{-1}$, high current on/off ratios of $>10^5$, and low subthreshold swing values of ~75 mV dec^{-1} at room temperature. Bi_2SeO_5 can also be selectively etched away while keeping the underlying Bi_2O_2Se nearly unchanged.

Lattice and band structure of Bi_2O_2Se and Bi_2SeO_5

As illustrated in Fig. 1a, layered Bi_2O_2Se is an emerging high-mobility 2D semiconductor[31,32] that is a tetragonal system with I_4/mmm

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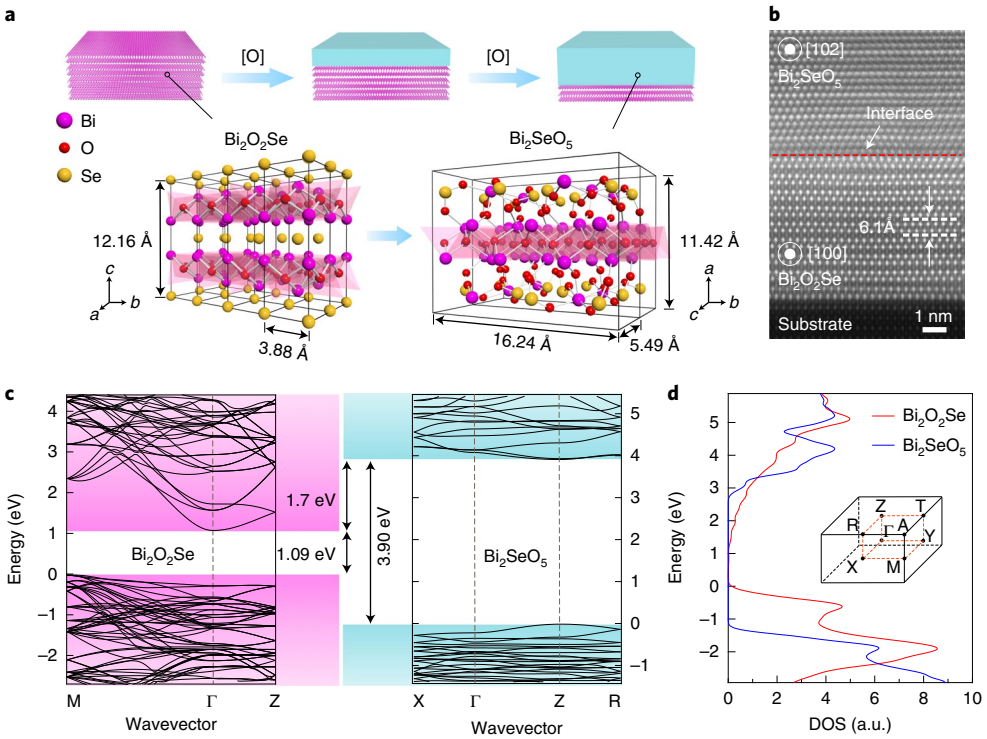

Fig. 1 | Crystal and electronic structures. a, Crystal structure of layered Bi_2O_2Se and its native oxide Bi_2SeO_5. Top: step-by-step oxidation of multilayer Bi_2O_2Se. **b**, Cross-sectional high-angle annular dark-field image of the Bi_2O_2Se/Bi_2SeO_5 heterostructure, showing an atomically sharp interface. **c**, Energy diagrams showing the band alignment between Bi_2O_2Se and Bi_2SeO_5. The band offsets are larger than 1 eV for both the CBM and VBM. **d**, Density of states of Bi_2O_2Se and Bi_2SeO_5 near the gap. The inset illustrates the first Brillouin zone of both materials.

space group ($a = b = 3.88$ Å, $c = 12.16$ Å, $Z = 2$) and is composed of positively charged $[Bi_2O_2]$ layers and negatively charged Se layers along the c axis. After thermal oxidation at elevated temperatures, more oxygen atoms intercalate into the structure, connecting all Se and Bi atoms into a network to form a dense Bi_2SeO_5 phase with *Abm*2 space group ($a = 11.42$ Å, $b = 16.24$ Å, $c = 5.49$ Å, $Z = 8$). Unlike ordinary metal oxides that constantly suffer from oxygen vacancies and variable valence of metals[20–30], the oxidation product of Bi_2O_2Se is a thermodynamically stable bismuth selenite Bi_2SeO_5 (Supplementary Fig. 1), where the valence state of bismuth is fixed at +3 and that of selenium at +4. The chemical equation of this reaction process is given by

$$Bi_2O_2Se + 3/2O_2 = Bi_2SeO_5 \quad (1)$$

Bi_2O_2Se can be converted gradually into Bi_2SeO_5 in a layer-by-layer manner, eventually forming a pure Bi_2SeO_5 phase (for details see Supplementary Figs. 1 and 2). An atomically sharp interface between the top Bi_2SeO_5 and underlying 2D Bi_2O_2Se layers was confirmed by cross-sectional scanning transmission electron microscopy of the heterostructure (Fig. 1b). We also performed ab initio calculations to investigate the band alignment between Bi_2O_2Se and Bi_2SeO_5. As shown in Fig. 1c, Bi_2O_2Se has a narrow indirect bandgap of 1.09 eV (close to ~0.8 eV, as measured by angle-resolved photoemission spectroscopy[32]) with a valence band maximum (VBM) at the X point and conduction band minimum (CBM) at the Γ point, whereas Bi_2SeO_5 has a much wider bandgap of ~3.9 eV with both the CBM and VBM at the Z point. More importantly, the energy band offset between these two materials is 1.7 eV for the CBM and 1.1 eV for the VBM, respectively, which satisfies the criterion for the band offset (>1 eV) for a practical gate dielectric to minimize leakage current. The calculation was further verified experimentally by ultraviolet photoelectron spectroscopy (Supplementary Fig. 3; for more details of theoretical calculations see Supplementary Figs. 4–6).

Controlled oxidation and selective etching

To optimize the Bi_2O_2Se/Bi_2SeO_5 heterostructure, we systematically investigated the thermal oxidation behaviour of 2D Bi_2O_2Se crystals synthesized by chemical vapour deposition on mica substrates. We used optical microscopy to monitor the morphological evolution of the Bi_2O_2Se nanoplates under thermal treatment in air (Supplementary Fig. 2). The Bi_2O_2Se nanoplates are shown to undergo significant changes in transparency while maintaining their shape, indicating an enlarged bandgap. Atomic force microcopy (AFM) showed that the surfaces of Bi_2O_2Se after thermal oxidation remain atomically smooth, with an expected height expansion. As seen in Fig. 2a, by carefully adjusting the oxidation temperature in the range of 370–400 °C, the thickness of a four-layer Bi_2O_2Se nanoplate shows a linear relationship with respect to the oxidation time in the first 20 min. Notably, the sample thickness increases by ~0.2 nm per layer until all four layers of Bi_2O_2Se are converted to Bi_2SeO_5, beyond which the sample thickness is saturated. Based on the unit cell volume and coordination number Z, an increase of 0.24 nm in thickness is expected along the c axis when one layer of Bi_2O_2Se (thickness of 0.61 nm) is converted into Bi_2SeO_5 (Fig. 2a, insets), consistent with our experimental observations. At higher temperatures, the oxidation process is significantly accelerated so that thicker oxide layers can also be achieved (Supplementary Fig. 7). It is worth noting that, despite its reactivity at elevated temperatures, Bi_2O_2Se is stable under ambient conditions (Supplementary Figs. 8 and 9).

In the modern semiconductor industry, selective etching of SiO_2 plays a key role in the creation of very-large-scale integrated circuits. Bi_2SeO_5 can also be selectively etched over Bi_2O_2Se by using diluted

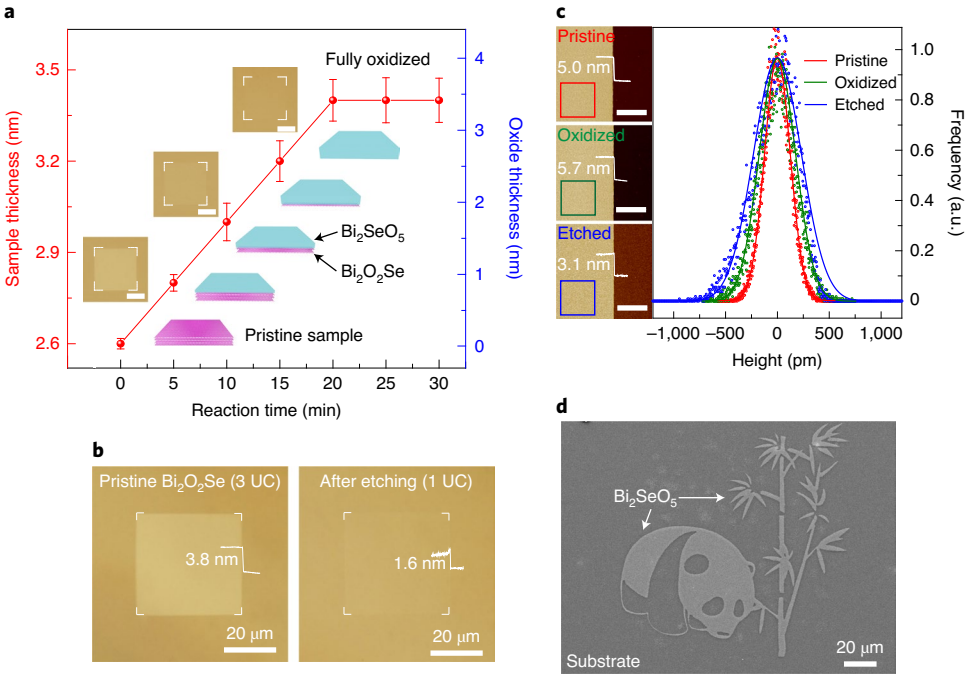

Fig. 2 | Controlled oxidation of Bi_2O_2Se layers and facile etching of Bi_2SeO_5. **a**, Time-dependent oxidation of Bi_2O_2Se, showing a linear relationship between the sample thickness and oxidation time. After 20 min, the 2D Bi_2O_2Se nanoplate is completely converted into Bi_2SeO_5. Inset images above the red line: optical microscopy images of the pristine Bi_2O_2Se nanoplates (bottom), after 10 min oxidation (middle) and after 20 min oxidation (top). Scale bars, 10 μm. Inset images below the red line: layer-by-layer oxidation model of four-layer Bi_2O_2Se nanoplates (L, layer). **b**, Optical microscopy images of a 3-unit-cell-thick (3-UC) Bi_2O_2Se nanoplate before oxidation and etching (left) and a 1-UC Bi_2O_2Se nanoplate obtained after oxidation and etching (right). **c**, Height and surface roughness measurements of a pristine Bi_2O_2Se nanoplate (red), Bi_2O_2Se/Bi_2SeO_5 after oxidation (green) and the thinned Bi_2O_2Se nanoplate after etching of the top Bi_2SeO_5 (blue). Standard deviations within the colour-coded areas in the corresponding AFM images (left), taken as a measure of surface roughness, are ~1.0 (pristine), ~1.3 (oxidized) and ~1.6 Å (etched). Scale bars, 5 μm. **d**, Scanning electron microscopy (SEM) image of a complex Bi_2SeO_5 pattern after selective-area etching. A high spatial resolution of ~1 μm can be deduced from the thinnest bamboo branches in the etched pattern.

HF acid (0.2%). The selectivity of HF etching is estimated to be greater than 100 (Supplementary Fig. 10), which is satisfactory when compared with the wet etching of SiO_2. For example, a 3-unit-cell (3-UC) Bi_2O_2Se nanoplate can be reduced to a single unit cell after oxidation and HF etching (Fig. 2b). More importantly, as illustrated in Fig. 2c (see Supplementary Fig. 11 for details), the surface of 2D Bi_2O_2Se nanoplates remains ultra-smooth, even after thermal oxidation (standard deviation of roughness $R_a \approx 1.3$ Å) and subsequent etching ($R_a \approx 1.6$ Å), showing only a slight increase of surface roughness compared with the pristine Bi_2O_2Se ($R_a \approx 1.0$ Å). Using selective etching and standard electron-beam lithography, complicated patterns (such as a giant panda) can be fabricated (Fig. 2d). The spatial resolution of this pattern (~1 μm) is superior to that of wet etching of SiO_2 (ref. [4]).

Dielectric properties

To evaluate the potential of Bi_2SeO_5 as a gate dielectric, we measured the dielectric properties of Bi_2SeO_5 thin films thermally oxidized from Bi_2O_2Se grown on Nb-doped $SrTiO_3$ substrates. The device configuration for capacitance–voltage (C–V) measurements is shown in Fig. 3a and Supplementary Fig. 12, where ~20-nm-thick Bi_2SeO_5 film is sandwiched between the top Au electrode and the conductive Nb-$SrTiO_3$ substrate. The relative permittivity of Bi_2SeO_5 is calculated by

$$C = A\varepsilon_0\varepsilon_r/d \quad (2)$$

where C is the measured capacitance, ε_0 is the vacuum permittivity, ε_r is the relative permittivity, A is the area of the Au electrode and d is the thickness of the Bi_2SeO_5. Figure 3a shows that, for a d.c. bias ranging from −2.5 V to 2.5 V, ε_r stays at ~21 with no discernible fluctuations, indicating that Bi_2SeO_5 is a stable high-κ dielectric (κ, dielectric constant). Temperature-dependent measurements show that Bi_2SeO_5 retains its high-κ nature from 80 to 330 K (Fig. 3b), with little variation near room temperature (280–330 K). For oxide thickness below 20 nm, the C–V measurements based on metal–insulator–metal structures become difficult due to the relatively large leakage current at high biases. To this end, we performed quantitative microwave impedance microscopy (MIM)[33] to determine the thickness-dependent dielectric constant of Bi_2SeO_5 at ~3 GHz. As shown in Fig. 3c (see Supplementary Fig. 13 for details), the microwave permittivity of Bi_2SeO_5 stays at around 21 and only decreases slightly for thicknesses below 5 nm, which corresponds to an equivalent oxide thickness (EOT) as small as 0.9 nm. The persistence of high κ into the microwave regime and ultrathin limit is compelling for high-speed electronic applications and will continue to be explored in our future work.

Another important factor for evaluation of a gate dielectric is the leakage current, which contributes to the static power consumption of an integrated circuit and should be kept below a certain level. For the device in Fig. 3a, the measured leakage current of Bi_2SeO_5 is lower than 1×10^{-7} A cm^{-2} under an external field strength of 1 MV cm^{-1} (Fig. 3d), which meets the criteria for most demanding dynamic random access memory applications[2]. For an external field as high as 2 MV cm^{-1}, the leakage current of Bi_2SeO_5 is still several orders of magnitude smaller than the low-power limit and standard

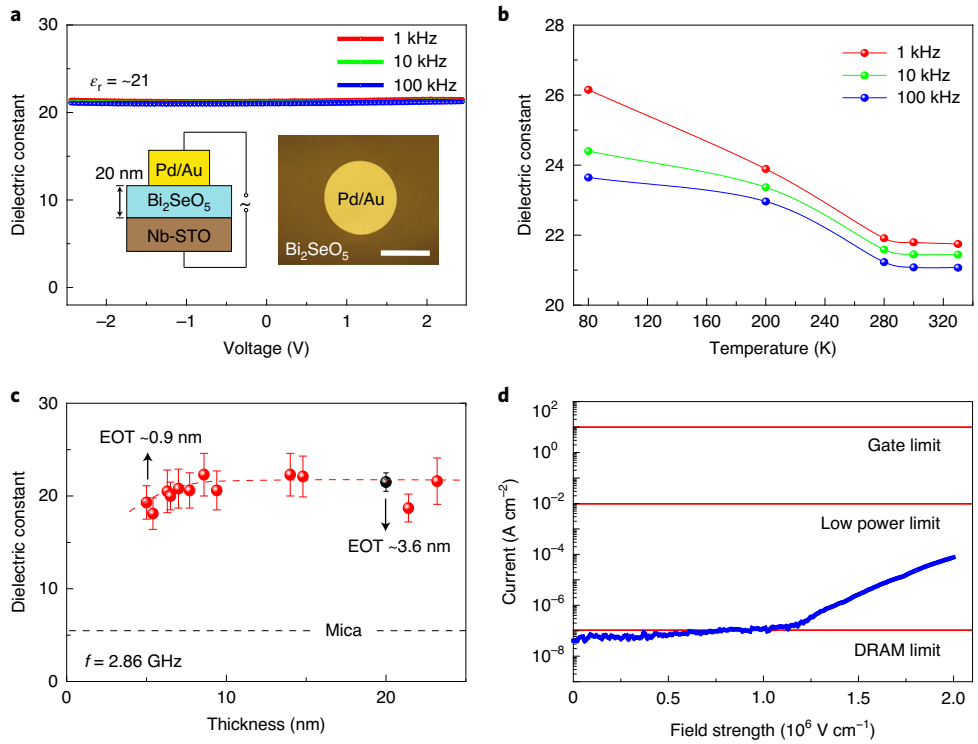

Fig. 3 | Electrical properties of Bi_2SeO_5. **a**, Bias-dependent dielectric constant calculated from *C*–*V* curves of a Bi_2SeO_5 metal–insulator–metal device at three different frequencies. The insets show the layer structure and an optical image of the device. Scale bar, 200 μm. **b**, Temperature-dependent dielectric constant of Bi_2SeO_5 measured at three different frequencies. **c**, Thickness-dependent dielectric constant of Bi_2SeO_5 at 2.86 GHz measured by MIM. The permittivity of the mica substrate is indicated in the plot. The dielectric constant value of the 20-nm sample in **a**, measured at 100 kHz by the *C*–*V* method, is included as a black data point for comparison. **d**, Leakage current as a function of the electric field strength of the Bi_2SeO_5 device in **a**. Horizontal red lines mark the limits of leakage current for various types of integrated circuit. DRAM, dynamic random access memory.

complementary metal–oxide–semiconductor gate limit. This gate leakage of Bi_2SeO_5 is comparable to that of thermal SiO_2 with the same EOT of ~3.6 nm.

FETs and inverter circuits

The exquisite electrical properties of Bi_2SeO_5 and its compatibility with microprocessing facilitate the fabrication of top-gated Bi_2O_2Se FETs with its native oxide as the gate dielectric (Fig. 4a and Supplementary Fig. 14). Here, Fe/Au were used for the source and drain electrodes to form ohmic contacts to the 2D Bi_2O_2Se. For gate electrodes, we used Pd/Au to match the work function between Pd (5.1 eV) and Bi_2O_2Se (~5.1 eV). As shown in Fig. 4b, the output characteristics of a Bi_2O_2Se FET with ~20-nm-thick Bi_2SeO_5 native gate dielectric (EOT ≈ 3.6 nm) exhibit typical n-type behaviour with a linear I_{ds}–V_{ds} at low bias and saturation at high bias, indicative of negligible Schottky barriers at the source and drain metal contacts. Room-temperature transfer curves at different V_{ds} show a steep rise of drain current with a subthreshold slope of ~75 mV dec^{-1} (Supplementary Fig. 15), approaching the thermal limit of ~60 mV dec^{-1} at 300 K. Compared with devices with HfO_2 as the top gate, Bi_2O_2Se/Bi_2SeO_5 FETs exhibit much weaker hysteresis between forward and reverse gate sweeps in transfer curves (Supplementary Fig. 16), signifying the presence of a clean semiconductor–oxide interface. Meanwhile, the I_{on}/I_{off} of this device (>10^5) meets the standard for practical logic circuits (10^4) with no obvious drift in the threshold voltage. The maximum apparent field-effect mobility in our Bi_2O_2Se/Bi_2SeO_5 FETs is over 300 cm^2 V^{-1} s^{-1} while maintaining a moderate threshold voltage of approximately −1 V (Supplementary Fig. 17). To accurately demonstrate the intrinsic mobility of Bi_2O_2Se with native gate oxide Bi_2SeO_5, Hall-effect measurements will be required in the future.

Taking advantage of the facile patterning technique, we are able to fabricate simple logic circuits based on Bi_2O_2Se/Bi_2SeO_5 FETs (Supplementary Fig. 18). Figure 4d illustrates the most essential NOT gate (also known as an inverter), which operates between 0 V (logic state 0) and 1 V (logic state 1) with a voltage gain as high as 150. To our knowledge, this large voltage gain exceeds previously reported devices based on 2D and other nanostructured semiconductors[34,35].

To demonstrate the scaling potential of Bi_2SeO_5 as gate dielectrics, we fabricated top-gated Bi_2O_2Se FETs with ~5 nm Bi_2SeO_5 as the native gate oxide (EOT ≈ 0.9 nm), showing I_{on}/I_{off} ≈ 10^5, an apparent field-effect mobility of ~250 cm^2 V^{-1} s^{-1}, a subthreshold swing of less than 75 mV dec^{-1} and a breakdown voltage larger than 8 V (Supplementary Fig. 19). Other FETs with thinner gate dielectrics (EOT < 0.9 nm) and logic gates or even integrated circuits may also be fabricated by using a similar protocol in the future.

Conclusions

We have reported the fabrication of FET devices in which an atomically thin high-mobility semiconductor channel material (Bi_2O_2Se) is integrated with a native oxide high-κ gate dielectric (Bi_2SeO_5). Our approach can create an atomically sharp and chemically clean semiconductor–oxide interface, as illustrated by the low hysteresis of the devices. The high dielectric constant and robustness of Bi_2SeO_5 also offers considerable scaling potential, down to an EOT of 0.9 nm. This material system, which supports selective etching and scalable patterning, provides an opportunity to adapt existing silicon-based semiconductor technology to high-mobility 2D materials.

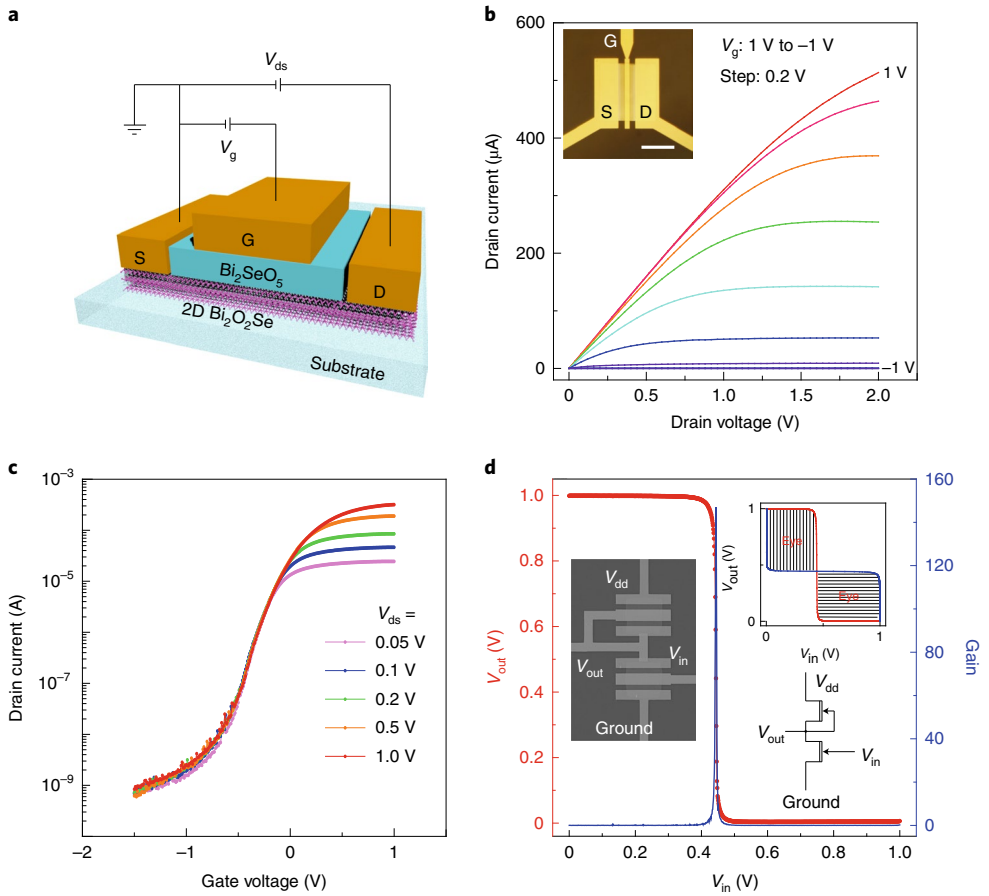

Fig. 4 | Top-gated Bi_2O_2Se/Bi_2SeO_5 FETs and inverter circuit. a, A 3D illustration of a Bi_2O_2Se FET with Bi_2SeO_5 as the gate dielectric. **b**, Output characteristics of a Bi_2O_2Se/Bi_2SeO_5 FET. Inset: optical microscopy image of the device. Scale bar, 20 μm. **c**, I_{ds}–V_g curves (transfer curves) of the FET, showing $I_{on}/I_{off} > 10^5$ and no appreciable drift in the threshold voltage. The extracted field-effect mobility of this device is 324 $cm^2 V^{-1} s^{-1}$. **d**, Voltage transfer characteristic (VTC) of an inverter, showing the output voltage as a function of input voltage (red) and its first derivative or the voltage gain (blue). The voltage gain of ~150 signifies large loading capacities for integrated circuits. Left inset: SEM image of a NOT gate composed of two Bi_2O_2Se/Bi_2SeO_5 FETs. Upper right inset: VTC (red line) and its mirrored curve (blue line). Lower right inset: equivalent circuit of the inverter. The shaded 'eyes' represent the noise margin of the inverter.

Methods

Synthesis of Bi_2O_2Se and Bi_2SeO_5 crystals. 2D Bi_2O_2Se crystals were synthesized using a procedure similar to that described in refs. [31,36]. Bi_2O_3 powder (Alfa Aesar, 5 N) and Bi_2Se_3 pieces (Alfa Aesar, 5 N) were placed separately in the hot zone centre and upstream area of a horizontal tube furnace and a 40-mm-diameter quartz tube. Freshly cleaved fluorophlogopite mica or strontium titanate (STO) was placed in the downstream area as the growth substrate. Argon or an argon–oxygen mixture (100 ppm oxygen) was used as the carrier gas to transport the vapour precursors to the cold region. Typical growth conditions were as follows. The source temperature was 600–620 °C and the substrate growth temperature was 480–550 °C. The system pressure was in the range of 100–1,000 torr and the carrier gas flow rate was 160–230 s.c.c.m. for argon and ~10–35 s.c.c.m. for the argon–oxygen mixture (100 ppm oxygen). The growth time ranged from 20 to 30 min. Bi_2SeO_5 was obtained by treating as-grown 2D Bi_2O_2Se crystals under an oxidation temperature of 370–400 °C in air.

As-grown 2D Bi_2O_2Se and Bi_2SeO_5 oxides were examined by optical microscopy (Olympus DX51 microscope), AFM (Bruker Dimension Icon with Nanoscope V controller) and X-ray diffraction (Rigaku D/Max-2000 diffractometer, Cu Kα radiation ($\lambda = 0.15406$ nm) at 40 kV and 100 mA).

Ab initio calculations. To resolve the band structure, we first performed ab initio calculations for Bi_2O_2Se and Bi_2SeO_5. Density functional theory calculations within the generalized gradient approximation (GGA) were performed using the Vienna ab initio simulation package with core electrons represented by the projector-augmented-wave potential[37]. Plane waves with a kinetic energy cutoff of 400 eV were used as the basis set. A k-point grid of 3 × 10 × 5 was used for Brillouin zone sampling. Geometry optimization was carried out until the residual force on each atom was less than 0.01 eV $Å^{-1}$. In addition, the Heyd–Scuseria–Ernzerhof (HSE) hybrid functional[38,39] (HSE06) was used for calculating the bandgaps. GGA gave an indirect bandgap of 0.45 eV for Bi_2O_2Se and a direct bandgap of 2.83 eV for Bi_2SeO_5, while HSE06 gave an indirect bandgap of 1.09 eV for Bi_2O_2Se and a direct bandgap of 3.90 eV for Bi_2SeO_5. We applied scissor corrections of 0.64 and 1.07 eV for Bi_2O_2Se and Bi_2SeO_5, respectively, to the corresponding GGA band structures according to the HSE06 gaps in Fig. 1c.

Metal–insulator–metal device fabrication and electrical measurements. The metal–insulator–metal capacitor shown in Fig. 3a was fabricated as follows. A continuous Bi_2O_2Se thin film grown on Nb-doped strontium titanate (Nb-STO) was fully oxidized into Bi_2SeO_5. Electron-beam lithography (EBL) was then used to write Pd/Au top electrodes (5/60 nm). Note that two layers of photoresist (conductive protective coating SX AR-PC-5000 and poly(methyl methacrylate) (PMMA)) were used to prevent charge accumulation on the insulating mica substrate during EBL.

Capacitance–voltage measurements were carried out on a semiconductor analyser (Keithley, SCS-4200) combined with a home-made cryogenic probe station covering the temperature range from 80 K to 330 K.

MIM measurements. The MIM experiment in Fig. 3c was carried out on a commercial AFM platform (Park AFM XE-70)[31]. For quantitative measurements, we used a tuning-fork-based probe[40] to simultaneously obtain the topography and microwave images (Supplementary Fig. 13). The demodulated MIM signals were then compared to the finite-element analysis (FEA) results to extract the dielectric constant at ~3 GHz.

Logic device fabrication and electrical transport measurements. Top-gate FETs were fabricated directly on as-grown nanoplates on an insulating mica substrate. Alignment marker arrays were first predefined onto the mica with standard photolithography techniques. These samples were then oxidized in a tube furnace to form a Bi_2O_2Se/Bi_2SeO_5 heterojunction. After that, the EBL process was used to create a PMMA mask that exposed the source/drain region of the FET devices. After 20 s of treatment with 0.2% HF solution, the top layer of Bi_2SeO_5 at

the source/drain region was removed. A second standard EBL process was then performed to deposit Pd/Au gate electrodes (5/60 nm). To finish the FET device fabrication, a third EBL process was subsequently carried out to deposit Fe/Au as the source and drain electrodes (5/60 nm).

The fabrication of inverter circuits was largely the same as the fabrication of the FET devices. To obtain the two identical FETs required for inverters, a single Bi_2O_2Se nanoplate was etched into two identical parts, using EBL-patterned PMMA as the mask and H_2SO_4/H_2O_2 solution as the etchant (10% H_2SO_4 + 10% H_2O_2)[41]. The subsequent oxidation and electrode deposition processes were the same as for the FET device fabrication.

Electrical measurements of the top-gated FETs were carried out on a semiconductor analyser (Keithley, SCS-4200) combined with a micromanipulator 6200 probe station at room temperature under ambient conditions.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

H.P. conceived the original idea for the project. T.T. carried out the synthesis and structural characterizations of the bulk and 2D crystals. The devices were fabricated and measured by T.L., with help from L.X., Z.W., H.W. and R.J. H.F. and B.Y. carried out the theoretical calculations. The scanning transmission electron microscopy measurements were performed by Y.S. under the direction of P.G. MIM was performed by J.Y. under the supervision of K.L. The manuscript was written by H.P., T.L., T.T. and J.W. with input from the other authors. All work was supervised by H.P. All authors contributed to the scientific planning and discussions.

Competing interests

The authors declare no competing interests.

Additional information

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