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Impact of graphene interlayer on performance parameters of sandwich structure Pt/GaN Schottky barrier diodes

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Abstract

In this work, we have designed excellent performance GaN-based Schottky barrier diode (SBD) with a sandwich structure by inserting a graphene (Gr) interlayer. The electrical properties of Pt/Gr/GaN and Pt/GaN SBDs have been systematically investigated by the temperature-dependent current—voltage (I–V) and capacitance–voltage measurements in order to explore the effects of Gr on main diode parameters. At room temperature, the Pt/Gr/GaN SBD exhibited lower turn-on voltage (V_{on}), ideality factor (n), differential specific on-resistance (R_{on}), and higher Schottky barrier height (SBH), signifying enhanced device attributes. Furthermore, the ideality factor and SBH for the Pt/Gr/GaN SBD were found to be insensitive to temperature from the temperature-dependent I–V analysis. The results revealed a highly homogeneous Schottky barrier interface in the case of Pt/Gr/GaN SBD. This facile strategy opened a pathway to improve the performance of the nitride Schottky rectifiers.

Keywords: GaN, graphene, Schottky barrier diodes, ideality factor, Schottky barrier height

(Some figures may appear in colour only in the online journal)

1. Introduction

Due to its outstanding physical and chemical properties such as high intrinsic electron mobility, excellent chemical and mechanical stability, graphene (Gr) has been extensively used in applications for integration with other materials [1, 2]. When the Gr and the semiconductor surface come in close contact, a Schottky barrier is created due to the discrepancy in their work functions and the discontinuity in energy states. The Gr integration with semiconductors to form Schottky junction has been previously demonstrated in a variety of materials [3–10]. For nitride semiconductors, Tongay *et al* [11] investigated the rectifying behavior and thermal stability of Gr/GaN Schottky barrier diode (SBD) in 2011 first. They revealed that the Gr on n-GaN is a promising candidate for the Schottky devices. After that, several studies on Schottky contact between Gr and GaN or low aluminum AlGaN were reported [12–18].

In recent years, a new sandwich structure Schottky junction with a Gr interlayer between metal (M) and semiconductor (S) has been demonstrated. In M/Gr/S structure, the Gr interlayer directly transforms the physical and chemical nature of the interface, as well as the junction properties. However, the role of Gr as an interlayer on the attributes of a Schottky junction is still debatable. Some studies [19, 20] on M/Gr/Si Schottky junction revealed that the Gr interlayer considerably minimizes the interfacial reactions, and efficiently protects the

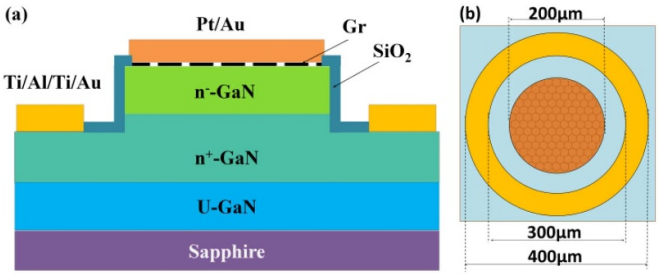

Figure 1. Schematic diagram of the quasi–vertical Pt/Gr/GaN SBD, (a) Side view and (b) Top view.

Schottky junction from unwanted changes in electrical properties. While other authors [21, 22] discussed the alleviation of the Fermi-level pinning effect and a significant reduction in Schottky barrier height (SBH) after Gr incorporation at the M/S interface. Nevertheless, the mechanisms of barrier formation and carrier transport at the M/Gr/S interface are still unclear, and only a few studies on M/Gr/GaN sandwich structure have been reported to date [23, 24].

In the present work, we fabricated quasi–vertical Pt/Gr/GaN SBD and systematically characterized the device performances in comparison with conventional Pt/GaN SBD. It is found that Pt/Gr/GaN SBD can realize lower turn-on voltage (V_{on}), differential specific on-resistance (R_{on}), lower ideality factor, and higher SBH simultaneously. Moreover, the homogeneity of the SBH is improved by Gr insertion layers. The excellent enhancement of device parameters might be attributed to the role of Gr interlayer which blocks the intermixing of Pt and GaN, which can reduce the formation of lower-barrier patches, thus improves the uniformity of the contact interface. The results indicate the enormous potential of Gr to be used as an interlayer in nitride Schottky rectifiers.

2. Experimental details

A schematic of the quasi-vertical Pt/Gr/GaN SBD is shown in figure 1. The GaN epilayers were grown by metal organic chemical vapor deposition (MOCVD) on (0001) sapphire substrate with a 0.2° off-cut angle. The epilayers consisted of a low-temperature GaN buffer layer, 3 μm thick unintentionally doped (UID) GaN layer, 1 μm thick Si heavily doped n^+-GaN ($\sim 10^{18}$ cm^{-3}) layer for ohmic contact, and finally 0.5 μm thick Si lightly doped n^-GaN ($\sim 10^{17}$ cm^{-3}) layer for Schottky contact.

The devices were fabricated using conventional photolithography and lift-off processes. First, the Schottky mesa area was defined by photolithography, and the n^-GaN layer around the mesa was etched by inductively coupled plasma (ICP) reactive ion etching. Here the mesa height is $\sim$0.85 μm, reaching down to the n^+-GaN layer. Subsequently, the ohmic contact regions were defined by the photolithography, and Ti/Al/Ti/Au (200 nm/1000 nm/700 nm/500 nm) stacks were formed using electron beam evaporation without thermal annealing. Prior to metal deposition, the samples were dipped in hydrochloric acid to remove native oxides from the surface. The dimensions

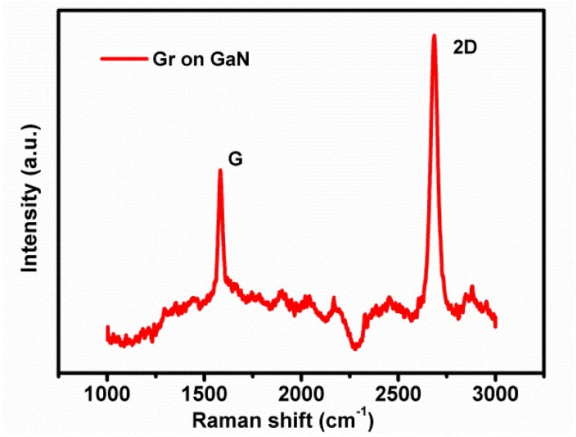

Figure 2. Raman spectrum of Gr transferred onto the n^-GaN.

of the circular ring contact are depicted in figure 1(b). After that, a 250 nm thick SiO_2 passivation layer was deposited on the device structures by plasma-enhanced chemical vapor deposition (PECVD). Following the photolithography step, circular windows for Schottky contact were opened by buffered oxide etchant (BOE) etching in the SiO_2 on top of the n^-GaN mesa. For Pt/Gr/GaN SBD fabrication, single layer Gr was transferred onto the patterned GaN surface. The mono layer Gr was grown on copper foil with chemical vapor deposition (CVD) method and transferred onto the GaN via wet transfer method with assistance of poly (methyl-methacrylate) (PMMA), which was finally etched away in acetone [25]. After another photolithography step, the Schottky contacts Pt/Au (30 nm/200 nm) metal stacks were deposited by electron beam evaporation. The oxygen plasma etching was employed to remove the Schottky metal-uncovered Gr. Finally, the ohmic contact windows were opened in the SiO_2 after lithography by BOE etching again. No field plate (FP) or edge termination technologies were employed in the devices. The Pt/GaN SBD were constructed by adopting the same procedures without Gr interlayer insertion. To investigate electrical properties, the current–voltage (I–V) and capacitance–voltage (C–V) characteristics were measured using KEYSIGHT B1500 A semiconductor analyzer on a probe station with a controllable thermal chuck.

3. Results

Figure 2 illustrates the Raman spectroscopy of the Gr on the n^-GaN. The primary in-plane vibrational mode of G peak at 1581 cm^{-1} and the double resonant D peak at 2684 cm^{-1} are observed. The peak intensity ratio of 2D and G is about 1.8, indicating its single layer property [15, 23]. The absence of the defect induced D-peak at near 1350 cm^{-1} implies the high crystalline quality of transferred Gr.

The ohmic contacts of the Pt/Gr/GaN devices were characterized by a circular transmission line model (CTLM). A contact resistivity ρ_c of 1.7×10^{-5} Ω cm^2 and a sheet resistance R_{sh} of 66.7 Ω sq^{-1} are extracted through the linear fitting of the resistance versus ln(R/r) as shown in the inset of figure 3. The

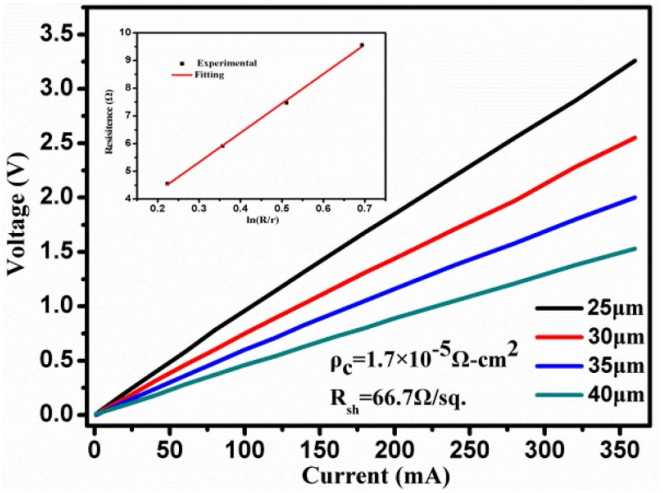

Figure 3. *I–V* characteristics of the ohmic contact for Pt/Gr/GaN SBD for various dimensions of circle radius. The inset shows the resistance versus ln(*R*/*r*), where *R* is the radius of the outer circle, and *r* is the radius of the inner circle.

Pt/Gr/GaN SBD reveals excellent ohmic behavior as shown in figure 3.

Figure 4(a) plots the *I–V* and ideality factor *n* versus voltage (*n–V*) characteristics for Pt/Gr/GaN and Pt/GaN SBDs. The current values of Pt/GaN and Pt/Gr/GaN SBDs at 2 V are 46 mA and 85 mA, respectively. By linear extrapolation of the *I–V* curve, the turn-on voltage (V_{on}) of the SBDs is obtained. For the SBD with Gr interlayer, V_{on} value of around 0.73 V is noticed, which is lower than that of 0.81 V for the SBD without Gr interlayer. The ideality factor *n* can be extracted according to the formula (1) [26],

$$n = \frac{q}{kT}\frac{1}{dlog\,(I)\,/dV} \tag{1}$$

where *q* is the electron charge, *k* is the Boltzmann constant, and *T* is the measured temperature. From the ideality factor *n* versus low voltage plots, it can be seen that the ideality factor of Pt/Gr/GaN before turn-on is smaller than that of Pt/GaN, which is 1.13 and 1.47 at the low bias of 0.35 V, respectively. The ideality factor *n* is the critical parameter to evaluate the junction quality. Usually, the non-uniformity of the Schottky junction interface leads to the inhomogeneity of the SBH, which is the main reason for the *n* becoming larger [27]. The obvious reduction in the value of the ideality factor indicates that Gr insertion layer in Pt/Gr/GaN SBD improves the Schottky interface quality and the homogeneity of the SBH.

Current density (*J*) and differential specific on-resistance (R_{on}) of the two types of SBDs as a function of voltage in log scale are presented in figure 4(b). Current on/off ratio as high as near 10^9 is achieved for both SBDs. The subthreshold slope (SS) is extracted to be 67 mV dec^{-1} for Pt/Gr/GaN SBD and 88 mV dec^{-1} for Pt/GaN SBD, signifying refined Schottky interface quality and better rectifying behavior due to Gr incorporation.

For the relatively heavily doping of the active layer and no field plate or edge termination processes, it can be seen

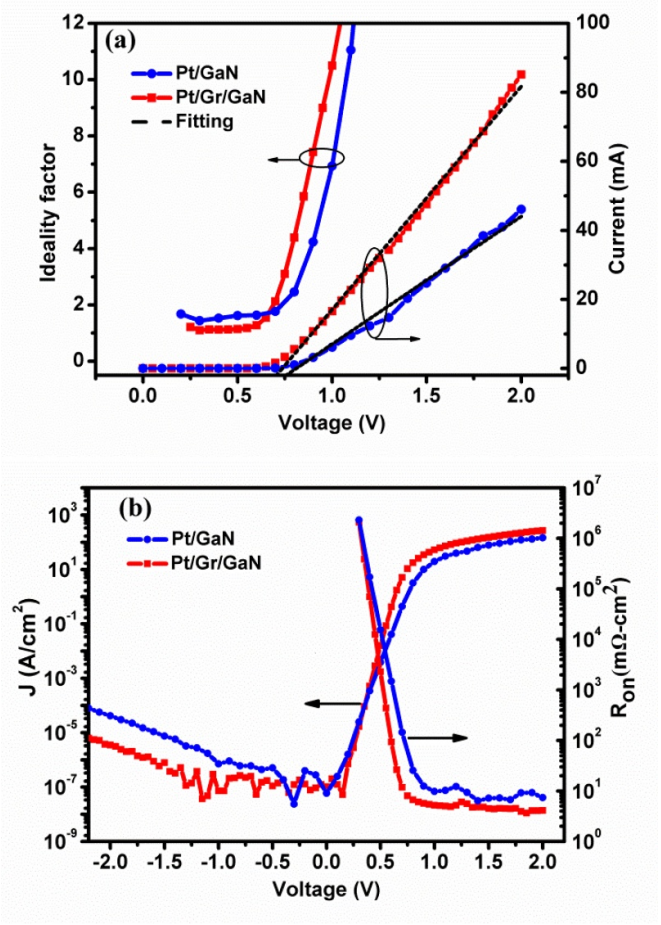

Figure 4. (a) Forward *I–V* and *n–V* characteristics of Pt/Gr/GaN and Pt/GaN SBDs in linear scale. The linear fitting is also plotted to extract the V_{on} values. (b) *J–V* and forward R_{on}–*V* characteristics in log scale.

that the leakage of the devices under reverse bias is high for both SBDs. The leakage current measured at −2 V was 3.54×10^{-6} A cm^{-2} for Pt/Gr/GaN SBD, which is over one order of magnitude lower than that of 4.19×10^{-5} A cm^{-2} for Pt/GaN SBD. Gr interlayer, as a diffuse barrier, blocks the metal and semiconductor intermixing, which can induce low barrier patches and result in leaky channels [20, 27, 28]. Therefore, the reduction of leaky channels due to the Gr interlayer makes the leakage smaller.

According to the thermionic emission model, the *I–V* relationship can be expressed as [11]:

$$I = I_s exp\,(qV/nkT - 1) \tag{2}$$

$$I_s = AA^*T^2 exp\,(-\phi_B/kT) \tag{3}$$

where I_s is the reverse saturation current, ϕ_B is the Schottky barrier height, *A* is the contact area, A^* is the Richardson constant (26.4 A cm^{-2} K^{-2} for GaN). The ϕ_B is determined to be 0.91 eV and 0.83 eV for the Pt/Gr/GaN and Pt/GaN

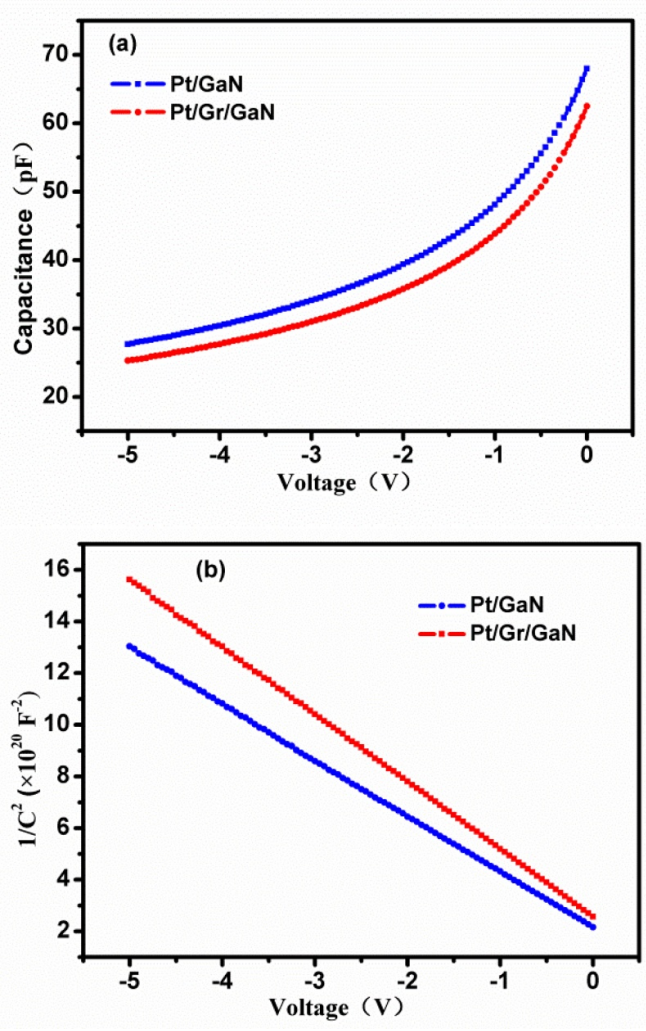

Figure 5. (a) *C–V* and (b) $1/C^2$–*V* characteristics of Pt/GaN and Pt/Gr/GaN SBDs.

junction, respectively. The higher ϕ_B of the Pt/Gr/GaN, in comparison with junction without Gr interlayer, implies better Schottky property is achieved at the contact interface. It is noted that the Pt/Gr/GaN SBD exhibits lower V_{on} and higher SBH. This is due to the lower ideality factor of Pt/Gr/GaN with more homogeneity junction interface. The R_{on} as a function of voltage is plotted in log scale, as shown in figure 4(b). At the same current density of 145 A cm^{-2}, R_{on} is calculated to be 4.3 mΩ-cm^2 and 7.4 mΩ-cm^2 for Pt/Gr/GaN and Pt/GaN SBDs, respectively. The decrease of R_{on} in Pt/Gr/GaN devices might be associated to the alleviated Schottky contact resistance for the excellent conductivity and electronically transparent properties of the Gr interlayer.

For further investigation, the *C–V* characteristics were recorded at 1 MHz frequency, as plotted in figure 5(a). It can be observed for both samples that the measured capacitance of the *C–V* curve is dominated by the metal/semiconductor interface, which is in accumulation region near zero bias. With an increase in negative voltage, the device enters the depletion region, which correlates with the decreasing capacitance. It is noticeable that Pt/Gr/GaN SBD exhibits the lower value of capacitance than Pt/GaN SBD. In order to determine the built-in voltage V_{bi} and net doping concentration N_D of devices, the Mott-Schottky plot $(1/C^2–V)$ analysis is employed following the equation [29]:

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_0\varepsilon_r N_D}(V_{bi} - V - kT/q) \tag{4}$$

where ε_0 is the permittivity of vacuum, ε_r is the relative permittivity of GaN, and V_{bi} is the built-in voltage of the device. The net concentrations N_D of Pt/Gr/GaN and Pt/GaN SBDs extracted from figure 5(b) are 5.98 × 10^{17} cm^{-3} and 7.18 × 10^{17} cm^{-3}, respectively. $V_{\rm bi}$ of the Pt/Gr/GaN is 1.02 V, and that of Pt/GaN SBD is 1.01 V.

In addition to the thermionic emission theory, Schottky barrier height ϕ_B can be likewise estimated from the *C–V* characteristics following the equations [29]:

$$q\phi_B = qV_{bi} - q\phi_{IL} + (E_C - E_F) \tag{5}$$

where ϕ_{IL} is the image-force-induced barrier height lowering, E_C is the bottom of the conduction band, and E_F is the Fermi level. ϕ_{IL} can be expressed as:

$$\phi_{IL} = \sqrt{qE_{SBD}/(4\pi\varepsilon_0\varepsilon_r)} \tag{6}$$

$$E_{SBD} = \sqrt{2qN_D V_{bi}/(\varepsilon_0\varepsilon_r)} \tag{7}$$

and

$$E_C - E_F = kT\ln(N_C/N_D) \tag{8}$$

where E_{SBD} is the electric field at the Schottky contact interface and N_C is the effective density states in conduction band. According to these formulas, ϕ_B is extracted to be 0.99 eV for Pt/Gr/GaN SBD and 0.97 V for Pt/GaN SBD. A higher value of ϕ_B for junction with Gr interlayer compared to the interface without Gr interlayer is observed, which is consistent with the *I–V* measurements. It is also notable that the difference between $\phi_{B,C-V}$ (ϕ_B obtained from *C–V*) and $\phi_{B,I-V}$ (ϕ_B obtained from *I–V*) for Pt/Gr/GaN SBD is 0.08 eV, while that is 0.14 eV for Pt/GaN SBD. Unlike the *I–V* characteristics, the *C–V* characteristics are not influenced by the potential fluctuations of the barrier height [5]. Therefore, the $\phi_{B,I-V}$ value is closer to the $\phi_{B,C-V}$ in case of Pt/Gr/GaN SBD, suggesting a more spatially homogeneous Schottky barrier. The parameters of these two SBDs obtained from *I–V* and *C–V* characteristics are summarized in table 1.

The energy band diagram of Pt/Gr/GaN structure is shown in figure 6. In the case of Pt/GaN, the height of the Schottky-barrier is almost independent of metal work-function due to the strong Fermi-level pinning at interface. In the case of Pt/Gr/GaN, when the Pt is deposited on the Gr surface, a new type of contact of Pt/Gr layer is formed. Because Pt work function of 5.65 eV is much larger than the Gr work function of 4.5 eV [5], electrons move from Gr to metal and results in Fermi levels of Gr to shift downwards with respect to the conical point by ΔE_F. A dipole layer is formed at the interface

Table 1. Summary of device parameters for Pt/Gr/GaN and Pt/GaN SBDs.

Sample	N_D (10^{17} cm^{-3})	V_{on} (V)	n	R_{on} (mΩ-cm^2)	$\phi_{B,I-V}$(eV)	$\phi_{B,C-V}$ (eV)
Pt/Gr/GaN	5.98	0.73	1.13	4.36	0.91	0.99
Pt/GaN	7.18	0.81	1.47	7.64	0.83	0.97

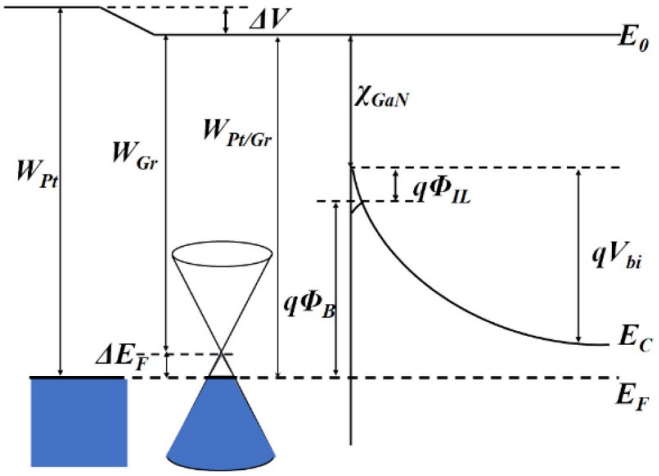

Figure 6. Energy band diagram of Pt/Gr/GaN heterostructure.

of Pt and Gr due to the electron transfer, which results in a potential step (ΔV). The formation of dipole layer will affect SBH of the interface. As shown in the energy-band diagram, the work function $W_{Pt/Gr}$ can be extracted as $W_{Pt/Gr} = W_{Pt}$-$\Delta V = W_G + \Delta E_F$. The ΔE_F is approximately 0.5 eV [30], so the value of $W_{Pt/Gr}$ is 5 eV. According to Schottky–Mott rule, $q\Phi_B = W_{Pt/Gr} - \chi_{GaN} = 0.9$ eV, which is very similar to the *I–V* measured SBH value of 0.91 eV for Pt/Gr/GaN SBD.

The forward *I–V* characteristics as a function of temperature from 25 °C to 145 °C are plotted in figure 7. At the subthreshold region, the forward current of the diodes at a fixed bias increases with rising the temperature for both types of SBDs whereas the V_{on} values shift to lower bias with increasing temperature. In the insets of figures 7(a) and (b), the linear Richardson plots (J/T^2 versus $1/kT$) obtained from the *I–V–T* data are drawn, which indicate the forward current limitation of the devices by thermionic emission. Based on expressions of (2) and (3), the values of ideality factor n and ϕ_B at each temperature are extracted using thermionic emission model in figure 7(c). For Pt/GaN SBD, it is noted that the ideality factor decreases from 1.47 to 1.16 while the barrier height increases from 0.83 eV to 0.95 eV with the temperature increasing from 25 °C to 145 °C. This behavior of the temperature dependence of the ideality factor is the so-called T_0 anomaly. It is believed that lateral inhomogeneity of the contact results in the T_0 anomaly [31], which can be described as a function of $n = 1 + T_0/T$, where T_0 is a constant related to the barrier distribution. The temperature dependent behavior of barrier height is also evidence that can be explained by the inhomogeneous nature of Schottky barrier for the lower-barrier patches at the M/S interface [32]. For the Pt/Gr/GaN SBD, ideality factor n shows very weak temperature dependence in the range of 1.13–1.18, and

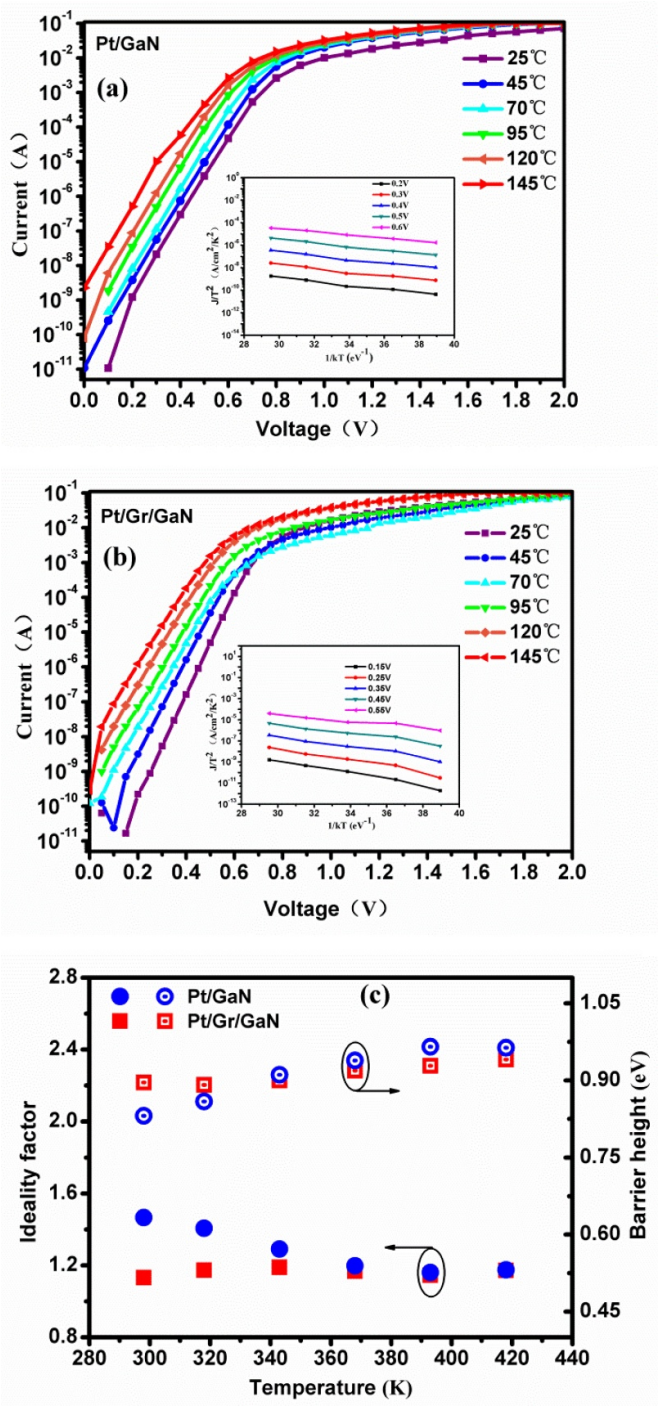

Figure 7. Forward *I–V* characteristics as a function of temperature for (a) Pt/GaN SBD and (b) Pt/Gr/GaN SBD. The insets show Richardson's plot derived from the forward *I–V–T* data. (c) Ideality factor and SBH as a function of temperature.

the ϕ_B also shows slight fluctuation with increasing temperature. The T_0 of Pt/Gr/GaN is smaller than that of Pt/GaN, so at

low temperature, the difference of n between Pt/Gr/GaN and Pt/GaN is large and they become closer with the increase of temperature. It is noted that the barrier height of Pt/GaN is higher than that of Pt/Gr/GaN at high temperature. From the relation $\emptyset_B(T) = \emptyset_{B0} - \frac{q\sigma_\emptyset^2}{2kT}$, where$\sigma_\emptyset$ is the standard deviation of the barrier height distribution, and Φ_{B0} is the ideal barrier [31], it can be extracted that the Φ_{B0} and $\sigma_\emptyset$ of Pt/GaN is higher than that of Pt/Gr/GaN. The value of $\frac{q\sigma_\emptyset^2}{2kT}$ becoming smaller at high temperature makes the barrier height of Pt/GaN higher at high temperature. This signifies that an extremely homogeneous Schottky barrier interface is achieved with the Gr interlayer.

4. Conclusions

Pt/Gr/GaN and Pt/GaN SBDs are fabricated and characterized. The *I–V* and *C–V* characteristics demonstrate that the Pt/Gr/GaN SBD offers a smaller V_{on}, R_{on}, leakage current and ideality factor values, and a higher SBH in comparison with conventional Pt/GaN SBD. These attributes are associated to enhanced Schottky interface quality and rectifying performance by the Gr interlayer insertion. Temperature-dependent *I–V* results also reveal that a highly homogeneous Schottky barrier interface is achieved for Pt/Gr/GaN SBD. These phenomenal developments are ascribed to the fact that Gr interlayer blocks the intermixing of Pt and GaN, reduces the formation of lower-barrier patches, thus improves the uniformity of the contact interface. The obtained results suggest that Gr has great potential for use in the nitride Schottky rectifier.

Acknowledgments

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