NANO LETTERS
Cite This: Nano Lett. XXXX, XXX, XXX−XXX
Letter
pubs.acs.org/NanoLett

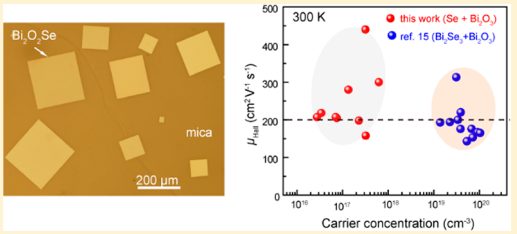
Low Residual Carrier Concentration and High Mobility in 2D Semiconducting Bi_2O_2Se

Jinxiong Wu,[†] Chenguang Qiu,[‡] Huixia Fu,[§] Shulin Chen,[∥,⊥] Congcong Zhang,[†] Zhipeng Dou,[∥,⊥] Congwei Tan,[#] Teng Tu,[†] Tianran Li,[†] Yichi Zhang,[†] Zhiyong Zhang,[‡] Lian-Mao Peng,[‡] Peng Gao,[∥,⊥] Binghai Yan,[§] and Hailin Peng*[,†,#]

[†]Center for Nanochemistry, Beijing Science and Engineering Center for Nanocarbons, Beijing National Laboratory for Molecular Sciences, College of Chemistry and Molecular Engineering, Peking University, Beijing 100871, P. R. China
[‡]Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing 100871, P. R. China
[§]Department of Condensed Matter Physics, Weizmann Institute of Science, Rehovot 7610001, Israel
[∥]Electron Microscopy Laboratory, School of Physics, Peking University, Beijing 100871, P. R. China
[⊥]International Center for Quantum Materials, Peking University, Beijing 100871, P. R. China
[#]Academy for Advanced Interdisciplinary Studies, Peking University, Beijing 100871, P. R. China

S *Supporting Information*

ABSTRACT: The air-stable and high-mobility two-dimensional (2D) Bi_2O_2Se semiconductor has emerged as a promising alternative that is complementary to graphene, MoS_2, and black phosphorus for next-generation digital applications. However, the room-temperature residual charge carrier concentration of 2D Bi_2O_2Se nanoplates synthesized so far is as high as about 10^{19}−10^{20} cm^{-3}, which results in a poor electrostatic gate control and unsuitable threshold voltage, detrimental to the fabrication of high-performance low-power devices. Here, we first present a facile approach for synthesizing 2D Bi_2O_2Se single crystals with ultralow carrier concentration of ∼10^{16} cm^{-3} and high Hall mobility up to 410 cm^2 V^{-1} s^{-1} simultaneously at room temperature. With optimized conditions, these high-mobility and low-carrier-concentration 2D Bi_2O_2Se nanoplates with domain sizes greater than 250 μm and thicknesses down to 4 layers (∼2.5 nm) were readily grown by using Se and Bi_2O_3 powders as coevaporation sources in a dual heating zone chemical vapor deposition (CVD) system. High-quality 2D Bi_2O_2Se crystals were fabricated into high-performance and low-power transistors, showing excellent current modulation of >10^6, robust current saturation, and low threshold voltage of −0.4 V. All these features suggest 2D Bi_2O_2Se as an alternative option for high-performance low-power digital applications.



KEYWORDS: *Bi_2O_2Se, 2D materials, low residual carrier concentration, high mobility, field-effect transistor, chemical vapor deposition*

Carrier concentration and mobility are the two most primary parameters characterizing any semiconducting channel materials for digital applications. High carrier mobility of channel materials is used to accelerate the operating speed for high-performance digital devices.[1,2] Meanwhile, the low residual carrier concentration of the channel can induce excellent gate control (especially low threshold voltage), which is essential for lowering the operating voltage, thereby enabling the fabrication of low-power digital devices.[3−7]

High-mobility ultrathin semiconductors with excellent environmental stability are attracting extensive attention due to their potential application in next-generation electronics and photonics.[2,8−14] Very recently, Bi_2O_2Se,[15−21] a new air-stable and high-mobility two-dimensional (2D) semiconductor that is complementary to graphene,[22,23] MoS_2,[24,25] and black phosphorus,[26,27] was demonstrated as a promising semiconducting channel material with excellent switching behavior of I_{on}/I_{off} > 10^6 and high Hall mobility (up to 450 cm^2 V^{-1} s^{-1}) at room temperature. All these features match well with the requirements for fabricating high-performance Bi_2O_2Se transistors. However, the residual charge carrier concentration of 2D Bi_2O_2Se nanoplates synthesized so far is as high as ∼10^{19}−10^{20} cm^{-3} at room temperature, which results in poor electrostatic gate control as indicated by the really high threshold voltage (typically −7 V for a 6.2 nm thick 2D Bi_2O_2Se crystal).[15]

In the previous synthesis method of 2D Bi_2O_2Se nanoplates, Bi_2Se_3 and Bi_2O_3 were used as the coevaporation sources,

Received: September 12, 2018
Revised: November 12, 2018

DOI: 10.1021/acs.nanolett.8b03696
Nano Lett. XXXX, XXX, XXX−XXX

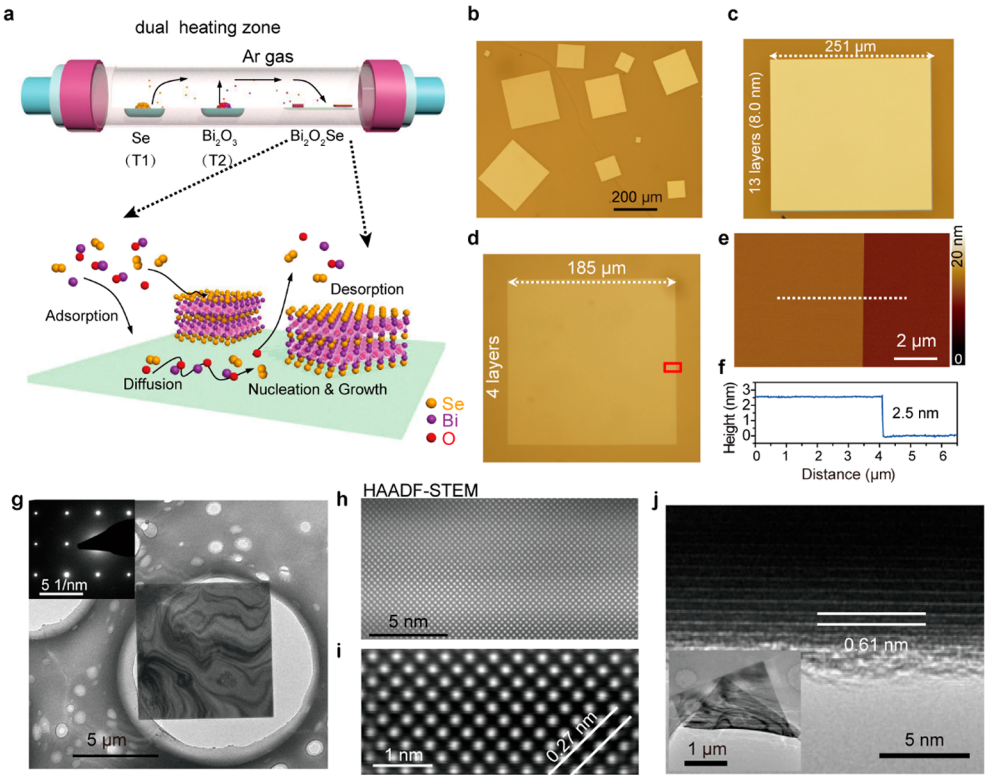


Figure 1. CVD growth and characterization of 2D Bi_2O_2Se crystals prepared by Bi_2O_3 selenization. (a) Schematic illustration of a CVD setup to synthesize Bi_2O_2Se nanoplates on mica using Se and Bi_2O_3 powders as coevaporation sources, which were separately located at the upstream and downstream heating zones, respectively. (b) Typical optical microscopy image of as-synthesized 2D Bi_2O_2Se crystals. (c) Bi_2O_2Se large single crystal, 8.0 nm thick (13 layers), with a domain size of 251 μm. (d) Ultrathin Bi_2O_2Se large single crystal with thickness down to 2.5 nm (4 layers) and lateral dimension of 185 μm. (e, f) Corresponding AFM image and height profile of the red-marked area in part d, showing a thickness of 2.5 nm. (g) Low-magnitude TEM image of a square Bi_2O_2Se nanoplate that transferred onto the TEM grid with PMMA and dilute HF-assisted method. The selected area electron diffraction pattern (inset) reveals the single crystallinity of as-synthesized Bi_2O_2Se. (h, i) Atomically resolved scanning TEM image of the Bi_2O_2Se nanoplate, consistent with the atomic arrangements of the *ab* plane in tetragonal Bi_2O_2Se. (j) High-resolution TEM image recorded from the folded edge of a Bi_2O_2Se nanoplate (inset), showing a clear layer space of 0.61 nm.

which involves very complex elementary processes. For example, the bulk Bi_2Se_3 would be mainly decomposed by following the formula $Bi_2Se_3(s) = 2BiSe(g) + 1/2Se_2(g)$ at the beginning, whereas its decomposition would be altered greatly after a long period of heating.[28] This feature might be detrimental to the synthetic reproducibility and defect control of 2D Bi_2O_2Se crystals, giving rise to a high residual carrier concentration.

In the present work, 2D large single crystals of Bi_2O_2Se were readily grown by using the simple substances of Se elements and Bi_2O_3 powders as coevaporation sources. Remarkably, with optimized synthetic conditions, as-synthesized 2D Bi_2O_2Se crystals showed ultralow carrier concentration of $\sim 10^{16}$ cm^{-3} and high Hall mobility up to 410 $cm^2 V^{-1} s^{-1}$ simultaneously at room temperature. High-performance and low-power transistors were fabricated on the basis of the high-quality 2D Bi_2O_2Se crystals, showing excellent current modulation of $>10^6$, robust current saturation, and low threshold voltage of -0.4 V. All these features suggest 2D Bi_2O_2Se crystals as an alternative option for low-power thin film transistor applications.

In the CVD growth process, reactive species are important factors that determine the growth results of 2D materials. The nature of the reactive species is the key factor that determines the concentrations and types of the decomposed precursors, which thermodynamically or kinetically determine whether such chemical reactions can occur. Therefore, by rationally choosing the reactive species to eliminate the possible side reactions or vacancies, one would obtain the desirable substances. In the present work, we chose the simple substances of Se element and Bi_2O_3 powder as the coevaporation sources to synthesize 2D Bi_2O_2Se crystals instead. Compared to the complex and variable decomposing reaction of Bi_2Se_3, Se source would mainly volatilize into the sole Se_2 molecules.[29,30] In this case, the chemical reaction would become much easier and show better controllability when a discretely controlled dual heating zone system was employed as indicated in Figure 1a. Note that the heating temperatures of Se and Bi_2O_3 are controlled independently, which are different from the previous one by employing Bi_2Se_3 and Bi_2O_3 in a sole heating zone (Figure S1). To this end, the relative partial pressure of the Se- and Bi-containing precursors can be altered continuously while changing the heating temperature of Se and Bi_2O_3 sources independently. With the optimized condition (for instance, optimal Se/Bi ratio), the defects or vacancies that contribute to the n-type conductivity of Bi_2O_2Se can be greatly depressed, thereby resulting in lower carrier concentration.[21]

Figure 1b shows the typical optical microscopy (OM) image of Bi_2O_2Se nanoplates grown on mica substrate, revealing a square-shaped morphology and a large average domain size of ~ 100 μm. With optimized growth conditions, ultrathin

DOI: 10.1021/acs.nanolett.8b03696
Nano Lett. XXXX, XXX, XXX−XXX

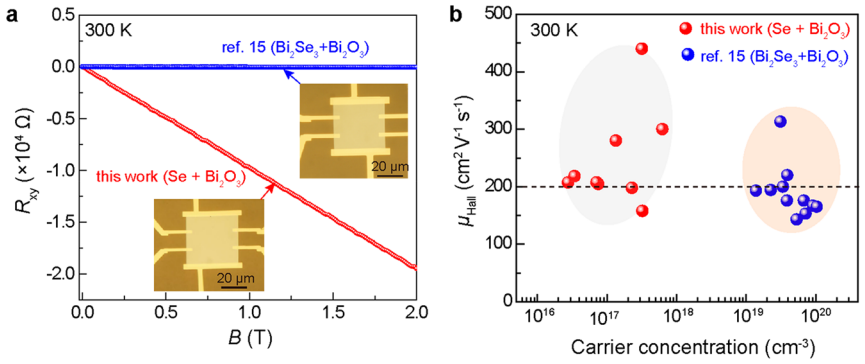


Figure 2. Room-temperature Hall measurements based on 2D nonencapsulating Bi_2O_2Se crystals. (a) Typical plot of the transverse Hall resistance R_{xy} versus an external magnetic field (B) for the Bi_2O_2Se crystals synthesized with an optimized Se + Bi_2O_3 method (red line), compared to the typical previously reported one (red line). Inset: the OM images of the fabricated Hall-bar Bi_2O_2Se devices both with a thickness of ~8.0 nm for easy comparison. (b) Statistics and comparison for Hall mobility and carrier concentration of 2D Bi_2O_2Se crystals, clearly indicating that the carrier concentration is lowered by 1−3 orders of magnitude while the Hall mobility still keeps a high average value of ~200 $cm^2\ V^{-1}\ s^{-1}$ on Bi_2O_2Se obtained from an optimized Bi_2O_3 selenization. For easy comparison, all the Bi_2O_2Se devices have similar thicknesses ranging from 6.0 to 9.0 nm.

Bi_2O_2Se large single crystals with domain sizes greater than 250 μm (Figure 1c) and thickness down to 4 layers (2.5 nm) can be readily obtained (Figure 1d−f), showing an ultrasmooth surface as indicated by the atomic force microscopy (AFM) measurements. As-grown Bi_2O_2Se nanoplates can be transferred onto the holey carbon-supported Cu grid for the characterization of transition electron microscopy (TEM) via a poly(methyl methacrylate)-mediated (PMMA-mediated) method (Figure 1g−j). As indicated in Figure 1g−i, the single-crystalline nature of Bi_2O_2Se was confirmed by selected area electron diffraction (SAED) and high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM). The well-defined lattice spacing of 0.28 nm matches well with the theoretical value (0.27 nm) of the (110) plane in Bi_2O_2Se (Figure 1i). With the top-view of the folded edge, we can obtain the cross-sectional information on a 2D material.[31] Evident from Figure 1j, a layer spacing of 0.61 nm along the [001] stacking orientation was observed in the folded region, corresponding to the layer thickness of Bi_2O_2Se (0.608 nm). Additionally, the elemental analysis, as indicated by the energy-dispersive X-ray spectroscopy (EDX), revealed a stoichiometric distribution of Bi, Se, and O (Figure S2). In short, high-quality ultrathin Bi_2O_2Se crystals were readily obtained on mica substrate via a method of Bi_2O_3 selenization.

The synthetic recipes, such as growth temperature, can greatly affect the concentrations of precursors, and thus alter the conducting behavior of as-synthesized materials. To obtain the optimal Se/Bi recipes, we first kept the heating temperature of Se temperature constant (240 °C), and changed the heating temperature of Bi_2O_3 solely from 680 to 750 °C. In this case, different Se/Bi ratios can be readily obtained. The as-synthesized Bi_2O_2Se crystals were patterned into Hall-bar configurations, and Hall measurements were performed at room temperature. As shown in Figure S3, the carrier density of as-synthesized Bi_2O_2Se increased monotonously upon raising the heating temperature of Bi_2O_3, which suggests that a relatively low temperature of $T(Bi_2O_3)$ facilitates the synthesis of low-carrier-density Bi_2O_2Se. Therefore, for the purpose of low carrier density, the heating temperature of Bi_2O_3 was fixed at 680 °C in the present work, since very rare 2D Bi_2O_2Se crystals will be deposited on mica substrate when further lowering the heating temperature of Bi_2O_3.

With optimal Se/Bi ratio, the defects (such as Se vacancies) that contribute to the n-type conductivity of Bi_2O_2Se were greatly depressed presumably (Figure S4). To this end, we can achieve the synthesis of 2D Bi_2O_2Se crystals with the following two important characteristics: low residual charge carrier concentration and high mobility at room temperature, both of which are the most important metrics of a semiconductor for digital applications. As illustrated in Figure 2a, the transverse resistance R_{xy} was measured using the opposing contacts (V_2 and V_4, for example) perpendicular to the source-drain current path. The Hall coefficient R_H, defined as the slope of R_{xy} versus magnetic field B, reveals both the carrier concentration and sign of the charge carriers in a sample, according to the equation $n_{2D} = -1/eR_H$, where e is the charge of an electron, and n_{2D} is the 2D charge concentration. The as-synthesized Bi_2O_2Se showed a linear relationship and a negative slope of $R_{xy}-B$, suggesting an electron-dominated conducting behavior (n-type). However, with optimized synthetic conditions, the slope of $R_{xy}-B$ in the present work can be increased greatly compared to the previously reported one with a typical carrier concentration of $10^{13}-10^{14}$ cm^{-2} (Figure 2a). The much steeper slope of $R_{xy}-B$ clearly suggests a much lower residual carrier concentration.

To obtain a better understanding of the electrical properties, we performed the statistics for room-temperature Hall mobility of as-synthesized 2D Bi_2O_2Se crystals as a function of carrier concentration on multiple devices of different batches. As shown in Figure 2b, the previously reported 2D Bi_2O_2Se crystals exhibited a relatively high residual carrier concentration of $\sim 10^{19}-10^{20}$ cm^{-3} at room temperature. Such high carrier concentration is detrimental to digital applications for the poor electrostatic gate control, even when the channel thickness reaches the atomically thin limit. On the other hand, presumably because of decreased Se vacancies (Figure S4), CVD-grown Bi_2O_2Se crystals in our present work showed dramatically decreased residual carrier concentration by 2−3 orders of magnitude, whereas they maintained the high carrier mobility averaged at ~200 $cm^2\ V^{-1}\ s^{-1}$ and reached a peak value of 410 $cm^2\ V^{-1}\ s^{-1}$ at room temperature. This value is preferably comparable to the CVD-grown semiconducting transition metal dichalcogenides.[32,33] Notably, considering the small fluctuation of growth parameters and complex surface reactions during the CVD growth of different batches, it is

DOI: 10.1021/acs.nanolett.8b03696
Nano Lett. XXXX, XXX, XXX−XXX

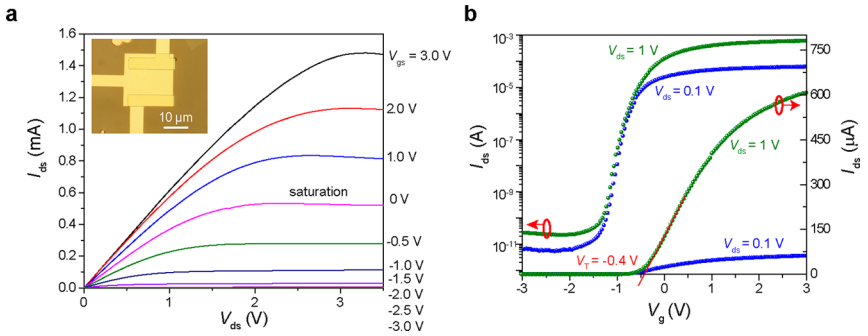


Figure 3. Top-gated 2D Bi_2O_2Se transistor with robust current saturation over a large voltage window and low threshold voltage. (a) Gate-dependent source-drain current (I_{ds}) as a function of source-drain voltage (V_{ds}), showing a robust current saturation over a wide voltage window. Inset: OM image of the fabricated top-gated 6.2 nm thick Bi_2O_2Se field-effect transistor. The device was fabricated on the mica substrate directly with 12 nm HfO_2 as top-gate dielectrics. (b) I_{ds} on a logarithmic (left side) and nonlogarithmic (right side) scale as a function of gate voltage obtained at room temperature, with drain-source voltages of 0.1 V (blue curve) and 1 V (green curve). Drain current modulation of $>10^6$ is observed on the electron side of gate doping, with a subthreshold swing of ~90 mV dec^{-1} and ultralow threshold voltage of −0.4 V. A slight turn-on at the hole side is also observed.

reasonable to observe small variations of carrier concentration ranging from 2×10^{16} to 7×10^{17} cm^{-3} (centered at $\sim 10^{17}$ cm^{-3}). The statistics for the carrier concentration and mobility of multiple 2D Bi_2O_2Se devices unambiguously demonstrated high carrier mobility and low residual carrier concentration simultaneously.

The high-quality ultrathin Bi_2O_2Se crystals with low residual carrier concentration and high carrier mobility facilitate the fabrication of high-performance and low-power field-effect transistors (FETs). Because of the excellent electrostatic control originating from a much depressed residual carrier concentration and ultrathin feature of the conducting channel, the top-gated Bi_2O_2Se FETs exhibit the following two remarkable boosts: current saturation over a large voltage window and low threshold voltage (V_{th}) of −0.4 V.

Current saturation is an important feature toward practical applications in digital displays and radio-frequency devices as they are operated in the saturation region.[23] As shown in Figure 3a, with the optimization of sample quality and device configurations, the current saturation over a large voltage window can be achieved in the relatively high drain-source bias (V_{ds}) region of the top-gated Bi_2O_2Se transistor (6.2 nm thick). Such saturation is elusive in graphene-based FETs because of the lack of a band gap,[23] and apparently different from the previously reported Bi_2O_2Se FETs with large threshold voltage (Figure S5). Additionally, the electrical contacts of Pd/Au (6/50 nm) remain ohmic in the linear region at low drain-source biases, thereby ensuring the high on-state conductance to some extent. Given the relatively long channel length of 10 μm, the on-state current, another key metric in transistors, can reach a high value of 70 $\mu A\ \mu m^{-1}$. This value is much higher than the typical value (<20 $\mu A\ \mu m^{-1}$) of multilayer-MoS_2-based FETs[24,34] and comparable to the highest value of several nm thick black-phosphorus-based FETs[27] with a channel length on the micrometer scale (Table S1). Note that substantial saturation current is expected if the channel length is shrunk approaching the nanometer scale, which needs further investigation.

The threshold voltage (V_{th}) of a field-effect transistor, one of the basic requirements for low-power-consumption devices, is the minimum gate voltage (V_g) that is needed to create the conducting path between the source and drain terminals. As shown in Figure 3b, because of the much depressed residual carrier concentration, the 2D Bi_2O_2Se transistor can be switched on at a very low threshold voltage of ~−0.4 V, which is much lower than the previously reported value of ~−7 V in the Bi_2O_2Se-based FETs with similar thickness.[15] Meanwhile, the transfer curve shows a large on/off ratio of $>10^6$ in a very narrow V_g window, indicating a low subthreshold swing (SS) of ~90 mV dec^{-1} and off-state current of 10^{-10} A at the operating voltage of 1 V, both of which are key metrics for low-power devices. By linear fitting of the transfer curve based on the equation of $\mu_{app} = (L/W)(1/C_g)(dI_{ds}/dV_g)$, we can extract the two-probe apparent field-effect mobility as 202 $cm^2\ V^{-1}\ s^{-1}$, which is comparable to the typical value of Hall measurements, a method that is widely accepted to accurately reflect the intrinsic mobility of a material.[35,36]

In summary, high-mobility ultrathin semiconducting Bi_2O_2Se crystals were steadily prepared by a facile CVD method, which involved Bi_2O_3 and Se as the coevaporation source in the double heating zone. With optimized synthetic conditions, the 2D Bi_2O_2Se crystals showed lower carrier concentration by 2−3 orders of magnitude while retaining similar room-temperature mobility as reported for the previous samples. On the basis of these low-carrier-density samples, the threshold voltage of the Bi_2O_2Se field-effect transistor can be greatly depressed while keeping rapid switching behavior, which moves one step further toward the practical applications of low-power high-speed digital devices.

■ ASSOCIATED CONTENT

Supporting Information

Experimental details and supplementary figures. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b03696.

Additional experimental details and figures including schematic diagram, HAADF-STEM images, EDX analysis, carrier densities, Hall mobility, atomic structure, formation energy, and output curves (PDF)

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: hlpeng@pku.edu.cn.

DOI: 10.1021/acs.nanolett.8b03696
Nano Lett. XXXX, XXX, XXX−XXX

ORCID

Huixia Fu: 0000-0002-4498-6946
Zhiyong Zhang: 0000-0003-1622-3447
Hailin Peng: 0000-0003-1569-0238

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

We acknowledge financial support from the National Basic Research Program of China (2014CB932500, 2016YFA0200101, and 2014CB920900), the National Natural Science Foundation of China (21733001, 21525310, and 11774010), and China Postdoctoral Science Foundation Funded Project (Postdoctoral Innovative Talents Support Program). We gratefully acknowledge Electron Microscopy Laboratory in Peking University for the use of Cs corrected electron microscope.

■ REFERENCES

(1) Franklin, A. D. Nanomaterials in Transistors: From High-Performance to Thin-Film Applications. *Science* **2015**, *349*, aab2750.
(2) Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S. K.; Colombo, L. Electronics Based on Two-Dimensional Materials. *Nat. Nanotechnol.* **2014**, *9*, 768.
(3) Takagi, S.; Iisawa, T.; Tezuka, T.; Numata, T.; Nakaharai, S.; Hirashita, N.; Moriyama, Y.; Usuda, K.; Toyoda, E.; Dissanayake, S. Carrier-Transport-Enhanced Channel CMOS for Improved Power Consumption and Performance. *IEEE Trans. Electron Devices* **2008**, *55*, 21−39.
(4) Gonzalez, R.; Gordon, B. M.; Horowitz, M. A. Supply and Threshold Voltage Scaling for Low Power CMOS. *IEEE J. Solid-State Circuits* **1997**, *32*, 1210−1216.
(5) Qiu, C. G.; Liu, F.; Xu, L.; Deng, B.; Xiao, M. M.; Si, J.; Lin, L.; Zhang, Z. Y.; Wang, J.; Guo, H.; Peng, H. L.; Peng, L. M. Dirac-Source Field-Effect Transistors as Energy-Efficient, High-Performance Electronic Switches. *Science* **2018**, *361*, 387−391.
(6) Jain, A.; Alam, M. A. Proposal of a Hysteresis-Free Zero Subthreshold Swing Field-Effect Transistor. *IEEE Trans. Electron Devices* **2014**, *61*, 3546−3552.
(7) Chhowalla, M.; Jena, D.; Zhang, H. Two-Dimensional Semiconductors for Transistors. *Nat. Rev. Mater.* **2016**, *1*, 16052.
(8) Bandurin, D. A.; Tyurnina, A. V.; Yu, G. L.; Mishchenko, A.; Zolyomi, V.; Morozov, S. V.; Kumar, R. K.; Gorbachev, R. V.; Kudrynskyi, Z. R.; Pezzini, S.; Kovalyuk, Z. D.; Zeitler, U.; Novoselov, K. S.; Patane, A.; Eaves, L.; Grigorieva, I. V.; Fal'ko, V. I.; Geim, A. K.; Cao, Y. High Electron Mobility, Quantum Hall Effect and Anomalous Optical Response in Atomically Thin InSe. *Nat. Nanotechnol.* **2017**, *12*, 223−227.
(9) Oyedele, A. D.; Yang, S.; Liang, L.; Puretzky, A. A.; Wang, K.; Zhang, J.; Yu, P.; Pudasaini, P. R.; Ghosh, A. W.; Liu, Z. $PdSe_2$: Pentagonal Two-Dimensional Layers with High Air Stability for Electronics. *J. Am. Chem. Soc.* **2017**, *139*, 14090−14097.
(10) Zhao, Y.; Qiao, J.; Yu, Z.; Yu, P.; Xu, K.; Lau, S. P.; Zhou, W.; Liu, Z.; Wang, X.; Ji, W. High-Electron-Mobility and Air-Stable 2D Layered $PtSe_2$ FETs. *Adv. Mater.* **2017**, *29*, 1604230.
(11) Zhang, W.; Huang, Z.; Zhang, W.; Li, Y. Two-Dimensional Semiconductors with Possible High Room Temperature Mobility. *Nano Res.* **2014**, *7* (12), 1731−1737.
(12) Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S. Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012**, *7*, 699.
(13) Liu, Y.; Duan, X.; Huang, Y.; Duan, X. Two-Dimensional Transistors Beyond Graphene and TMDCs. *Chem. Soc. Rev.* **2018**, *47*, 6388−6409.
(14) Wang, F.; Wang, Z.; Yin, L.; Cheng, R.; Wang, J.; Wen, Y.; Shifa, T. A.; Wang, F.; Zhang, Y.; Zhan, X.; He, J. 2D Library Beyond Graphene and Transition Metal Dichalcogenides: a Focus on Photodetection. *Chem. Soc. Rev.* **2018**, *47*, 6296−6341.
(15) Wu, J.; Yuan, H.; Meng, M.; Chen, C.; Sun, Y.; Chen, Z.; Dang, W.; Tan, C.; Liu, Y.; Yin, J.; Zhou, Y.; Huang, S.; Xu, H. Q.; Cui, Y.; Hwang, H. Y.; Liu, Z.; Chen, Y.; Yan, B.; Peng, H. High Electron Mobility and Quantum Oscillations in Non-Encapsulated Ultrathin Semiconducting Bi_2O_2Se. *Nat. Nanotechnol.* **2017**, *12*, 530−534.
(16) Wu, J.; Tan, C.; Tan, Z.; Liu, Y.; Yin, J.; Dang, W.; Wang, M.; Peng, H. Controlled Synthesis of High-Mobility Atomically Thin Bismuth Oxyselenide Crystals. *Nano Lett.* **2017**, *17*, 3021−3026.
(17) Wu, J.; Liu, Y.; Tan, Z.; Tan, C.; Yin, J.; Li, T.; Tu, T.; Peng, H. Chemical Patterning of High-Mobility Semiconducting 2D Bi_2O_2Se Crystals for Integrated Optoelectronic Devices. *Adv. Mater.* **2017**, *29*, 1704060.
(18) Wu, M.; Zeng, X. C. Bismuth Oxychalcogenides: A New Class of Ferroelectric/Ferroelastic Materials with Ultra High Mobility. *Nano Lett.* **2017**, *17* (10), 6309−6314.
(19) Li, J.; Wang, Z. X.; Wen, Y.; Chu, J. W.; Yin, L.; Cheng, R. Q.; Lei, L.; He, P.; Jiang, C.; Feng, L. P.; He, J. High-Performance Near-Infrared Photodetector Based on Ultrathin Bi_2O_2Se Nanosheets. *Adv. Funct. Mater.* **2018**, *28*, 7.
(20) Yin, J.; Tan, Z.; Hong, H.; Wu, J.; Yuan, H.; Liu, Y.; Chen, C.; Tan, C.; Yao, F.; Li, T.; Chen, Y.; Liu, Z.; Liu, K.; Peng, H. Ultrafast and Highly Sensitive Infrared Photodetectors Based on Two-Dimensional Oxyselenide Crystals. *Nat. Commun.* **2018**, *9*, 3311.
(21) Fu, H. X.; Wu, J. X.; Peng, H. L.; Yan, B. H. Self-Modulation Doping Effect in the High-Mobility Layered Semiconductor Bi_2O_2Se. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2018**, *97*, 5.
(22) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon films. *Science* **2004**, *306*, 666−669.
(23) Schwierz, F. Graphene Transistors. *Nat. Nanotechnol.* **2010**, *5*, 487−496.
(24) Desai, S. B.; Madhvapathy, S. R.; Sachid, A. B.; Llinas, J. P.; Wang, Q.; Ahn, G. H.; Pitner, G.; Kim, M. J.; Bokor, J.; Hu, C.; Wong, H. S. P.; Javey, A. MoS_2 Transistors with 1-Nanometer Gate Lengths. *Science* **2016**, *354*, 99−102.
(25) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147−150.
(26) Li, L.; Yu, Y.; Ye, G. J.; Ge, Q.; Ou, X.; Wu, H.; Feng, D.; Chen, X. H.; Zhang, Y. Black Phosphorus Field-Effect Transistors. *Nat. Nanotechnol.* **2014**, *9* (5), 372.
(27) Liu, H.; Neal, A. T.; Zhu, Z.; Luo, Z.; Xu, X.; Tománek, D.; Ye, P. D. Phosphorene: an Unexplored 2D Semiconductor with a High Hole Mobility. *ACS Nano* **2014**, *8*, 4033−4041.
(28) Porter, R. F.; Spencer, C. W. Stabilities of the Gaseous Molecules, BiSe, BiTe, and SbTe. *J. Chem. Phys.* **1960**, *32*, 943−944.
(29) Erdevdi, N.; Shpenik, O.; Markush, P. Excitation of Selenium Vapor by Slow Electrons. *Opt. Spectrosc.* **2015**, *119* (5), 799−804.
(30) Abowitz, G. Model of the Evaporation Kinetics from a Temperature-Programmed Large-Area Source. I. Pure Selenium. *J. Vac. Sci. Technol.* **1977**, *14* (3), 797−802.
(31) Meyer, J. C.; Geim, A. K.; Katsnelson, M. I.; Novoselov, K. S.; Booth, T. J.; Roth, S. The Structure of Suspended Graphene Sheets. *Nature* **2007**, *446* (7131), 60.
(32) Radisavljevic, B.; Kis, A. Mobility Engineering and a Metal−Insulator Transition in Monolayer MoS_2. *Nat. Mater.* **2013**, *12* (9), 815.
(33) Cui, X.; Lee, G.-H.; Kim, Y. D.; Arefe, G.; Huang, P. Y.; Lee, C.-H.; Chenet, D. A.; Zhang, X.; Wang, L.; Ye, F.; Pizzocchero, F.; Jessen, B. S.; Watanabe, K.; Taniguchi, T.; Muller, D. A.; Low, T.; Kim, P.; Hone, J. Multi-Terminal Transport Measurements of MoS_2

DOI: 10.1021/acs.nanolett.8b03696
Nano Lett. XXXX, XXX, XXX−XXX

Using a van der Waals Heterostructure Device Platform. *Nat. Nanotechnol.* **2015**, *10*, 534−540.
(34) Kim, S.; Konar, A.; Hwang, W.-S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J.-B.; Choi, J.-Y.; Jin, Y. W.; Lee, S. Y.; Jena, D.; Choi, W.; Kim, K. High-Mobility and Low-Power Thin-Film Transistors Based on Multilayer MoS_2 Crystals. *Nat. Commun.* **2012**, *3*, 1011.
(35) Choi, H. H.; Cho, K.; Frisbie, C. D.; Sirringhaus, H.; Podzorov, V. Critical Assessment of Charge Mobility Extraction in FETs. *Nat. Mater.* **2017**, *17*, 2.
(36) Fuhrer, M. S.; Hone, J. Measurement of Mobility in Dual-Gated MoS_2 Transistors. *Nat. Nanotechnol.* **2013**, *8* (3), 146.

DOI: 10.1021/acs.nanolett.8b03696
Nano Lett. XXXX, XXX, XXX−XXX